Petroleum Indicator by Electric Relaxation (PIER)

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1.0 INTRODUCTION

Real-time *measurement while drilling* (MWD) of the mud composition and flow rate at a drill bit is of significant importance to an oil well drilling operator. First of all, it could prevent a blowout when the drill bit unexpectedly encounters an oil reservoir (or the gas/water that is usually present with oil). On the other hand, it can indicate increased oil content when the drill bit is passing porous, oil-laden soil, that would be missed otherwise because of mud sealing the soil. A blowout typically damages drilling equipment and sometimes causes a fire, necessitating an expensive and dangerous recovery and/or rescue operations. The result of missing the oil is not as dramatic, but still costly. At the bottom of a drilling hole, the environment is extremely hostile, with pressures up to 20,000 psi and temperatures up to 175°C [1] challenging the MWD of the drilling fluid composition [1-4]. Therefore, existing methods of drilling fluid composition measurements, whether optical [1,2], acoustic [3], or microwave [4], are applied to samples after drilling or during break times. A means of measuring drilling fluid composition under extreme conditions **during oil drilling** would be extremely valuable [5], since it could significantly reduce the $1.5 billion a year losses when holes fail [6]. There is a strong demand for a composition measurement device that could operate *in situ* and in real-time, in the hostile downhole conditions, especially at depths of 5,000 feet or greater [5].

In response to this need, Physical Optics Corporation (POC) developed the novel *Petroleum Indicator by Electric Relaxation* (PIER) system, based on enhanced *dielectric spectroscopy* [7-9] for *in situ* real-time MWD of fluid composition and fluid flow. This is the first attempt to apply advanced dielectric spectroscopy to measuring fluid composition in the oil drilling environment. POC's PIER approach is based on the continuous time-domain measurement of the complex-value capacitance (and in turn of the dielectric polarization) of the fluid mixture of water/oil-based drilling mud, oil, natural gas, and other ingredients (such as brine) that flow through the PIER capacitance probe at the bottom of the hole near the drilling bit. The oil/mud fluid is measured dynamically because of the way the oil/mud fluid flow enters the PIER probe, which consists of two identical sensors arranged in series with the fluid flow. The fresh, unpolarized fluid continuously enters the first sensor, which contains a mixture of polarized and unpolarized material. But the fluid is uniformly polarized in the second sensor, due to the prepolarization in the first sensor, so this second sensor accurately measures the oil/mud composition, down to or even below 1% oil concentration. At the same time, the difference in the dynamics of polarization in the sensors is proportional to the flow rate.

The PIER system consists of four modules:

(A) PIER sensor head
(B) PIER signal acquisition electronic subsystem
(C) COTS wireless electromagnetic telemetry (WET) communication subsystem
(D) Surface electronics.

Subsystem (C) is integrated into subsystem (B). Subsystem (A) is located at the bottom of the drilling hole, attached to the first (pilot) segment of the drilling pipe; subsystem (B) is attached to the same segment of the drilling pipe but 5-25 m above subsystem (A), connected with (A) by wires. While the architecture of the PIER device includes wired communication between subsystems (A) and (B), wireless electromagnetic telemetry (WET) supports communication between (B) and (D).

In the course of this Phase II SBIR project, POC designed, assembled, and tested a fully functional PIER prototype (Figure 1-1). The tests conducted unambiguously demonstrated the capability of the prototype to measure the concentration of oil in the drilling mud in a wide range of oil concentrations. POC also conducted preliminary market analysis and identified potential users of the PIER technology who expressed interest in further improvement and commercialization of the technology. This report contains a detailed description of the PIER design and test results.

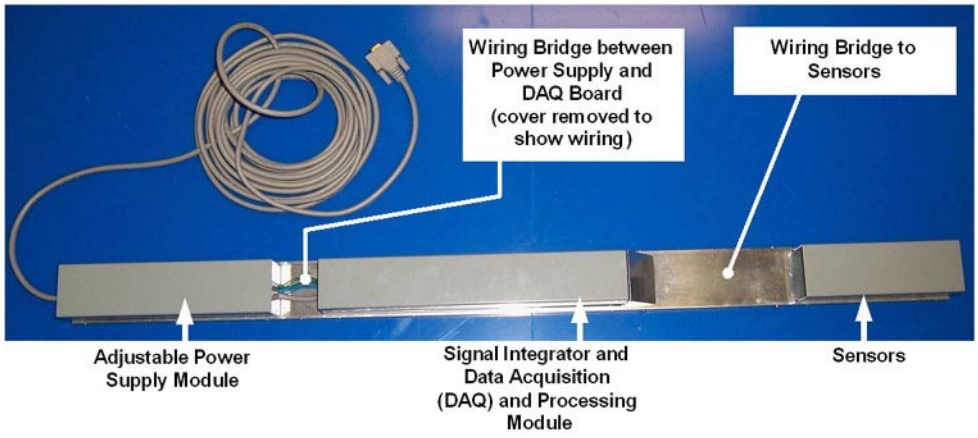


Figure 1-1
PIER prototype consisting of several modules located at the vicinity of (~0.5 m above) the drilling bit. The right module contains two capacitive sensors, the next module is a wire bridge to the sensor module, the next module contains electronic boards for signal integration, data acquisition, and data processing, while the left module contains the power supply (batteries). The sensor module is open for mud flow while other modules are hermetically sealed.

2.0 HIGHLIGHTS OF PHASE II ACHIEVEMENTS

In this Phase II project, POC developed a fully operational PIER prototype system that measures the oil content in drilling mud and the flow rate of this mud during drilling. It detects penetration of oil into the downhole and determines when the drill bit passes the oil-containing soil, thus allowing the operator to stop there or before reaching an oil reservoir. The overall goal of the Phase II PIER project was the design, fabrication, and demonstration of performance of the PIER Phase II prototype. This included the design and development of the PIER sensor head, signal-acquisition electronics, above-ground signal processing electronics, and integration with a wireless communication system between the sensor-head module and the ground to meet the Phase II technical objectives:

The following technical objectives were established for the Phase II work:

Objective 1. Optimize PIER System Architecture
Objective 2. Optimize PIER Sensor Head Module
Objective 3. Develop and Optimize the PIER Algorithms and Control/Interface Software
Objective 4. Design and Fabricate PIER Electronic Hardware and Pulse Generator
Objective 5. Integrate, Demonstrate and Test the Fully Functional PIER Prototype
Objective 6. Test the PIER Sensor under Field Conditions
Objective 7. Evaluate Applications and Commercial Scenarios for the PIER Technology.

In Phase II, these objectives were met and the following results were achieved:

- Determined the optimal parameters of all critical subsystems and of the overall system design, optimized the PIER sensor head physical structure, sensor signal acquisition electronics, above-ground signal processing electronics, and integration with the communication link between the sensor and the ground. Thus the PIER system was optimized to maximize measurement sensitivity and selectivity, as well as system environmental stability.
- Designed the *pipe-conformable* compact packaging, the structure of the electrodes, and the wired connection with the signal acquisition subsystem.
- Developed the data acquisition and processing algorithm to support PIER functionality. The data acquisition algorithm implemented in the programmable logic device (PLD) for fast (100 ns) data collection. Other functions (data processing and communication) based on the Microchip dsPIC30F6015 digital signal controller (dsPIC), which sets the measurement cycle, obtains data from PLD, and calculates drilling fluid composition (oil content) and flow rate. POC refined the time-domain-spectrometry Fourier-transform-based algorithm developed in Phase I, and created an advanced Fourier transform/cross correlation algorithm to identify the concentration level of oil in the mud.
- Developed all PIER electronic components as three functional PC boards: the adjustable power supply board generates voltage pulses of the needed magnitude and duration, the double-channel analog signal integrator (charge sensitive amplifier) converts the polarization current to the corresponding polarization charge, and the data acquisition module performs high-speed sampling and analog-to-digital conversion of the analog input signal. The latter monitors the analog signal and controls the power supply module to adjust the output voltage of the signal integrator.
- Integrated and tested the communication link for data transfer from the downhole PIER sensor head to the operator's interface.
- Integrated a fully functional PIER prototype and tested it under conditions simulating the downhole environment (vertical flow of the mud), evaluating its sensitivity and selectivity to oil in drilling mud. The prototype demonstrated the capability to measure oil concentration from <1% to practically 100%.
- Investigated near-term and longer-term application scenarios for PIER sensors. During this investigation POC contacted commercial partners, who expressed interest in PIER technology and may provide follow-on-funding.

3.0 PHASE II RESULTS

In Phase II, two variants of the PIER analog electronics were designed, fabricated, and evaluated. The first variant PIER I, contained only analog electronics, so a commercial, computer-based data acquisition board was used to digitize and transfer data to the computer for processing. This variant was tested, and a second version, PIER II, with embedded microcontroller, was developed as the result of optimization and partial redesign of PIER I. Both variants are described below.

3.1 Fourier Transform Algorithm for PIER

3.1.1 Data Acquisition and Processing

Time-domain spectrometry (TDS) is based on Borel's convolution theorem (BCT), which states that the product of Fourier transforms of two functions equals the Fourier transform of the convolution integral of these functions:

$$X^*(\omega)\cdot Y^*(\omega) = F\{x(t)\}_\omega \cdot F\{y(t)\}_\omega = F\left\{\int_{-\infty}^{\infty} x(t)y(t-\tau)d\tau\right\}\omega \quad . \qquad (3\text{-}1)$$

where $X^*(\omega) = F\{x(t)\}_\omega = \int_{-\infty}^{\infty} x(t)e^{-i\omega t}dt$

If the polarization current, *i(t)*, is additive and linearly proportional to the electric field, *E(t)*, and the electric field is considered as a sum of sequential short pulses, the resulting density of electric current, *j(t)*, can be expressed by the superposition of reactions, *g(t)*, to each short pulse of electric field with width *dt*:

$$j(t) = \int_0^t E(t-\tau)g(\tau)d\tau \quad , \qquad (3\text{-}2)$$

that is exactly the convolution integral for *E(t)* and *g(t)* and thus $j^*(\omega) = E(\omega)\cdot g^*(\omega)$. Because the electric current density is $j^*(\omega) = E(\omega)\cdot\sigma^*(\omega)$, the response function *g(t)* is the original function of the Fourier image for conductivity $\sigma^*(\omega)$. But the complex conductivity of the dielectric is $\sigma^*(\omega) = i\omega\varepsilon^*(\omega)$. Therefore the function *g(t)* is the integral of the original function for complex dielectric permittivity, $\varepsilon^*(\omega)$, according to the differential theorem for Fourier transform, $F\{f^{(r)}(t)\} = (ia)^{(r)}F\{f(t)\}$.

Another definition of dielectric permittivity, $D^*(\omega)=\varepsilon^*(\omega)E^*(\omega)$, connects the electric field, *E*, with the displacement field, *D*. This expression leads, according to BCT, to Duhamel's integral

$$D(t) = \varepsilon_0(\varepsilon_\infty E(t) + \int_0^t h(t)E(t-\tau)d\tau) \quad , \qquad (3\text{-}3)$$

where *h(t)* is the original function of Fourier image $\varepsilon^*(\omega)$ and ε_∞ is the very fast, optical part of dielectric permittivity. Because $D(t) = \varepsilon_0 q(t)$ if *q(t)* is the density of electric charge on electrodes, Eq. (3-3) can be significantly simplified in case of $E(t) = E_0 = Constant$:

$$h(t) = \frac{dq(t)}{dt}\cdot\frac{1}{\varepsilon_0 E_0} = i(t)\cdot\frac{1}{\varepsilon_0 E_0} \quad ; \qquad (3\text{-}4)$$

i.e., the function *h(t)* is proportional to the electric current, *i(t)* and, therefore, the function *g*(*t*) is proportional to the integral of this current, electric charge $q(t) = \int_0^t i(t)dt$. Therefore the electric charge on electrodes with area *S* at distance *d* is

$$Q(t) = q(t)S = \int_0^t V(t-\tau)I(\tau)d\tau \quad , \qquad (3\text{-}5)$$

where $V(t) = E(t)d$ is the electric voltage and $I(t) = j(t)S$ is the electric current.

The initial density of electric current, $j_k(0)$ and the saturating value for density of electric charge, $q_k(\infty)$, are related as $j_k(0) = q_k(\infty)/\tau_k$, where τ_k is the time constant of decay function $exp(t/\tau_k)$. Correspondingly, for the electric current integral, the polarization charge is

$$Q_0(t) = \int_0^t I(t)dt = V \sum_k a_k \int_0^t e^{\frac{t}{\tau}} dt = V \sum_k \left(\int_0^\infty q_k (1 - e^{-t/\tau_k}) d\tau \right) \quad , \tag{3-6}$$

where $a_k = q_k/\tau_k$. Thus the spectrum of the nonoptical part of dielectric permittivity, $\varepsilon^*(\omega)$, can be obtained by a Fourier transform of the electric charge

$$\varepsilon^*(\omega) = \frac{\varepsilon_0}{i\omega} F\{q(t)\}_\omega \quad . \tag{3-7}$$

In the PIER probe, the drilling fluid passes two equal capacitive sensors. If the same voltage is applied to both sensors, there is a difference in polarization currents in these sensors due to the flow of the fluid. In the first sensor, a dielectric moves through the capacitive cell at a rate of $du/dt = a$, where du is the change of volume. As a result, there is a supply of fresh (not yet non-polarized) dielectric and loss of the same volume of polarized material. The charge in the first sensor will, therefore, depend on the flow rate,

$$Q_1(t) = Q_0(t)(1 - \alpha t) + \sum_k \int_0^t a_k (1 - e^{-\frac{t-x}{\tau_k}}) dx \quad , \tag{3-8}$$

where the array of a_k represents amplitudes of polarization mechanisms of time constants τ_k. The polarization in the second sensor does not depend on the flow because the entering fluid, already polarized in the first sensor, compensates the loss of the fluid polarized in the second sensor. Thus, the charge in the second sensor is defined by Eq. (3-6).

We have simulated the PIER sensor's performance in MathCAD 2001 for two polarization times: $\tau 1 = 10^{-5}$ s and $\tau 2 = 5*10^{-4}$ s. The increment of polarization charge in both parts of the PIER sensor is shown in Figure 3-1.

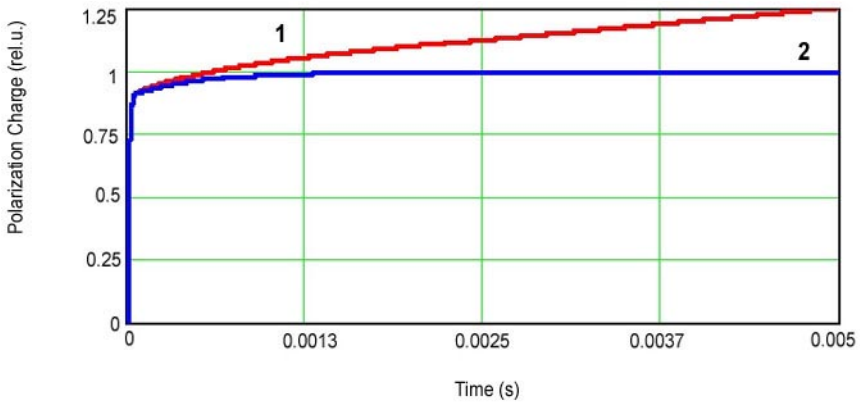


Figure 3-1
Increment of the polarization charge in time in the first (1) and second (2) parts of the PIER sensor (α = 50).

The parameter a is normalized to the volume of the sensor and means the rate of replacement per second. Figure 3-2 shows how the difference in full charges in first and second parts of the PIER sensor depends on the flow rate.

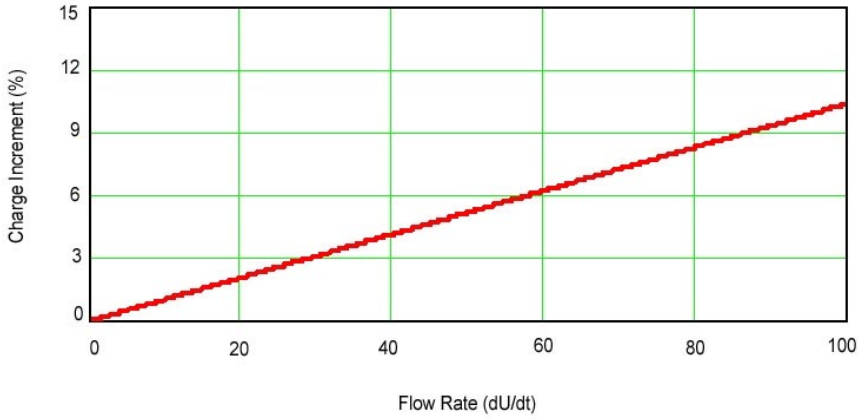


Figure 3-2
The charge increment between the first and second parts of the PIER sensor at various flow rates.

The linearity of the function in Figure 3-2 is clear. We also simulated the Fourier transform of the polarization charge in the second part of the sensor, which is defined by Eq. (3-6). The spectrum of complex dielectric permittivity obtained (incremental, nonoptical part) is presented in Figure 3-3.

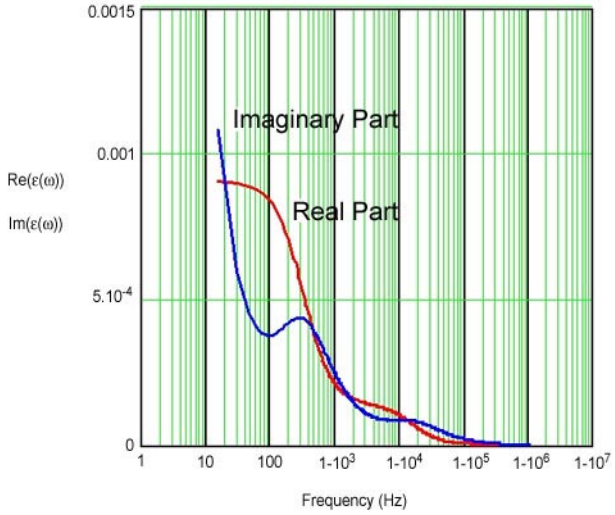


Figure 3-3
Incremental (nonoptical) component of the complex dielectric permittivity of material.

Two peaks of dielectric loss (the imaginary part of dielectric permittivity) are easy to detect. They are at f1 = 320 Hz and f2 = 16 kHz, which correspond to circular frequencies, $\omega = 2\pi f = 1/\tau$.

The differentiation of charges, $Q_1(t)$ and $Q_2(t)$, leads to the currents in sensors of,

$$i_2(t) = \int_o^\infty \frac{q(\tau)}{\tau} e^{\frac{t}{\tau}} d\tau \text{ and } i_1(t) = i_2(t)(1+\alpha t) \quad , \tag{3-9}$$

and the *flow rate* can be calculated as

$$U = \frac{\alpha}{S} = \frac{i_1(t) - i_2(t)}{i_2(t) * t * S} \quad , \tag{3-10}$$

where S is the cross-section of the flow. Because the result of the measurement of the flow rate does not depend on the distribution of the time constant, τ, if currents can be measured, the device can measure the flow rate for any fluid composition.

We have simulated the step-time of 0.5 μs and $2^{16} = 65536$ samples. This allowed us to calculate the spectrum in the range of about 20 Hz to 1 MHz and clearly determine both loss peaks.

3.1.2 Compact Algorithm of the Fast Fourier Transform

The limited capability of the microcontroller and energy consumption considerations do not allow use of the universal algorithm of the Fast Fourier Transform. No known simple algorithm of this transform provides enough data for the multicomponent spectrum. Nevertheless, dielectric spectrometry features the continuous rise of the transmitted charge, while the rate of this rise is continuously decreasing. This allows us to use the linear approximation of the time-domain input with varied time intervals between selected data. The exponential behavior of the input function naturally leads to the logarithmic increment of this interval. For example, if the initial time between data sampling is t_0 = 2 ns (as in our tests described in Section 3.0), doubling this interval for each following data picking step (i.e., $2t_0$, $4t_0$, $8t_0$ etc.) leads to the permanently small deviation of $Q(t)$ from the linear approximation at these intervals (see Figure 3-4). Thus the charge vs. time function can be linearly approximated at each of these intervals as

$$Q(t)_k^{k+1} = \frac{Q_{k+1} - Q_k}{t_0 2^k}(t - t_0 2^k) + Q_k \quad , \tag{3-11}$$

where Q_k and Q_{k+1} are measured at moments $t_0 2^k$ and $t_0 2^{k+1}$. The advantage of this method is the reduction in data array, reducing, for example, 1024 measurements to 10.

The next step in simplification is based on the permanent digitizing rate; i.e., t_0 has the same value for all measurements. Therefore all $t_0 2^k$ values will also be in the same, initially defined array. This allows use of the direct classic Fourier transform function

$$\int_0^\infty Q(t) e^{-j\omega t} dt = \sum_{k=0}^{\infty} \int_{t_k}^{t_{k+1}} Q(t) e^{-j\omega t} dt \quad , \tag{3-12}$$

where the summing can be interpreted as soon as the period of lowest frequency that is of interest is reached because of saturation of $Q(t)$. When $Q(t)$ becomes the constant, the increment of integral of Eq. (3-12) falls to zero.

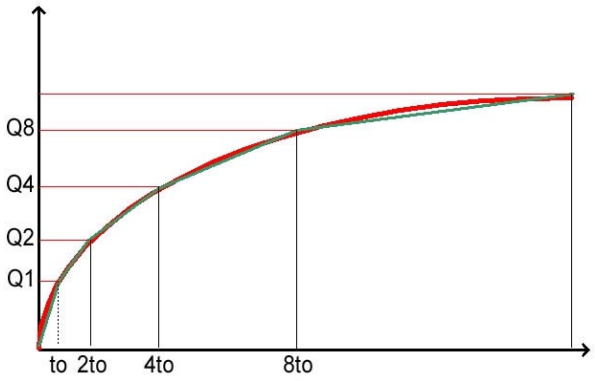


Figure 3-4
Linear approximation of polarization charge.

The application of Eq. (3-11) to Eq. (3-12) reduces the sum of integrals to the sum of definite numbers because resulting integrals

$$\int_{t_k}^{t_{k+1}} t^{e-j\omega t} dt \text{ and } \int_{t_k}^{t_{k+1}} e^{-j\omega t} dt \quad . \tag{3-13}$$

depend only on t_k and t_{k+1} values that are initially defined. Therefore, these integrals become numerical constants that can be calculated in advance and recorded in the controller memory. Thus the Fourier transform is reduced to the calculation of sum $\sum_k Q(t_k)a_k$.

The next simplification is related to the volume of transmitted data. The dielectric loss function can be described as a sum of Debye components [10,11]

$$\frac{A_i \omega \tau_i}{1+(\omega \tau_i)^2} \quad , \tag{3-14}$$

where A_i is an amplitude and τ_i is the time constant of polarization. In practice there are few peaks of dielectric loss or even a single peak. In this case A is the doubled magnitude of peak and τ is just a reverse circular frequency of the peak, $\omega^{-1} = (2\pi f)^{-1}$, where f is the frequency. Therefore the entire spectrum of dielectric loss can be reduced to one or a few parameters, A and τ. Specifically in the downhole application, where the spectrum range is initially defined, the single pair of parameters can work fine. This means that only two numbers can be transmitted to the surface electronics for every cycle of measurement.

3.1.3 Data Processing Algorithm

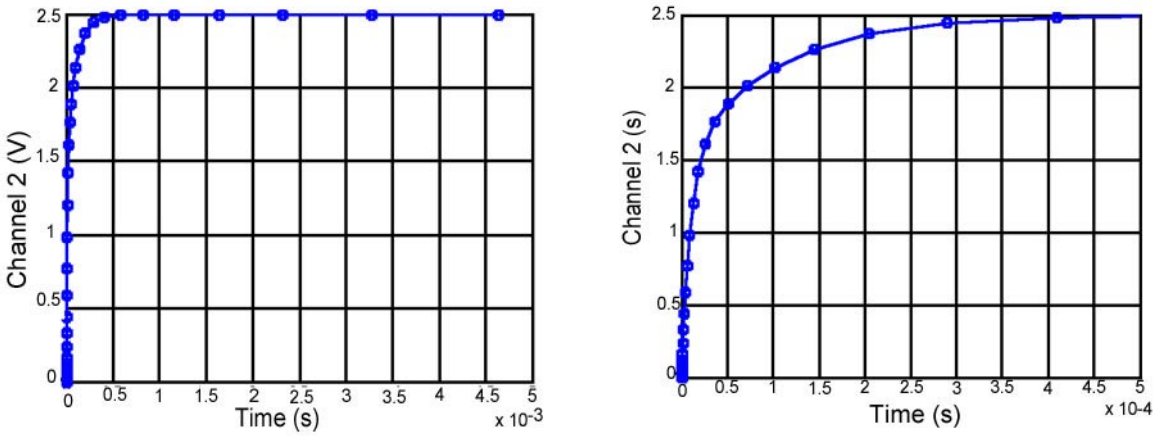
The data processing algorithm is illustrated using simulated data with numerical calculations performed in MATLAB. First, assume that the output from the signal integrator module can be represented as a sum of two exponentials:

$$y(t) = (\alpha_1 + \alpha_2) - \alpha_1 e^{\frac{-t}{\tau_1}} - \alpha_2 e^{\frac{-t}{\tau_2}} \quad . \tag{3-15}$$

For this example, assume that their amplitudes are of the same order of magnitude, while their time constants differ by a factor of ten. Let us use:

$$\begin{aligned} \alpha_1 &= 1 \qquad & \tau_1 &= 10^{-4} \\ \alpha_2 &= 1.5 \qquad & \tau_2 &= 10^{-5} \end{aligned} \quad . \tag{3-16}$$

Over 5 ms, this function is illustrated in Figure 3-5(a). Figure 3-5(b) presents the same function graphed from 0 to 0.5 ms. In either graph it appears the signal is a single exponential.



(a) (b)

Figure 3-5
Charge response with two polarization processes:
(a) Range from 0 to 5 ms; (b) Range from 0 to 0.5 ms.

Only a fraction of the thousands of samples taken at 10 MHz have actually been collected and used in processing. In this example, 50000 samples would be taken in 5 ms. Of these, just 32 samples, indicated by the blue circles in the graphs in Figure 3-5, are used in data processing.

Once all 32 samples have been stored, the frequency spectrum of $y(t)$, denoted, is generated. It is shown as curve (a) in Figure 3-6. From the frequency domain it is easy to identify the presence of two peaks, each of which is a bell-shaped curve corresponding to an exponential in the original function $y(t)$. In Figure 3-6 the peaks appear at approximately $f_1 = \log_{10}\left(\frac{1}{2\pi\tau_1}\right) = 4$ ($\log_{10}$ (Hz)) and $f_2 = \log_{10}\left(\frac{1}{2\pi\tau_2}\right) = 5$ ($\log_{10}$ (Hz)).

Having generated the frequency spectrum, the maximum value is easily identified, and this peak will correspond to one of the exponentials (at least approximately; it is unlikely one of the samples will coincide exactly with the maximum value).

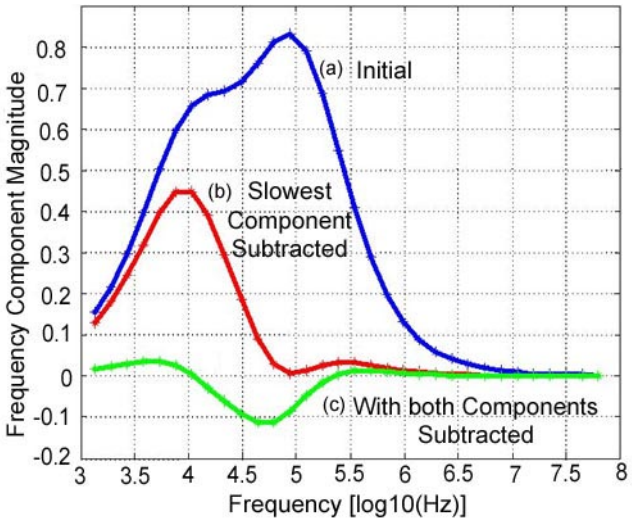


Figure 3-6
Frequency spectrum of *y(t)*, imaginary component.

In this example, the maximum value in the frequency domain is at $f_2' = 4.938(\log_{10}(Hz))$, at which point the spectrum has the value $\beta_2' = 0.832$. From f_2' and β_2' we generate time domain data corresponding to an exponential of amplitude $2\beta_2'$ and time constant $1/f_2'$ as follows:

$$y_2'(t) = 2\beta_2' e^{-t \cdot f_2'} \quad . \tag{3-17}$$

The calculated time domain data $y_2'(t)$ are then subtracted from the original time domain data *y(t)*, as in $\dot{y}(t) = y(t) - y_2'(t)$. The frequency spectrum of $\dot{y}(t)$, denoted $\dot{Y}(f)$, is then generated, shown as curve (b) in Figure 3-6. Note that $\dot{Y}(f = f_2')$ is approximately zero, as would be expected.

The peak in the red curve corresponds to parameters of the remaining exponential in the original time domain data, and can easily be identified. In this case $f_1' = 4.035\ \log_{10}\text{Hz}$ and $\beta_1' = 0.448$.

At this point, we have essentially found the amplitudes of the two exponential curves. However, in the frequency domain the two bell-shaped curves (one for each exponential) are superimposed (forming the blue curve above). Thus the peak of the blue curve is not precisely the peak of one of the underlying bell-shaped curves; the presence of the other bell-shaped curve adds to the peak we are trying to detect. The end result is that the amplitudes obtained do not correspond exactly to the amplitudes of the underlying exponentials. The errors introduced can be significant. The amplitudes can be connected by the following procedure.

We continue using the parameters corresponding to the curve (b) in Figure 3-6 by generating another set of time-domain data:

$$y_1'(t) = 2\beta_1'^{-t \cdot f_1'} \quad . \tag{3-18}$$

As before, we subtract this exponential from the remaining time data as follows: $\ddot{y}(t) = \dot{y}(t) - y_1'(t) = y(t) - y_1'(t) - y_2'(t)$. The frequency spectrum of $\ddot{y}(t)$, denoted $\ddot{Y}(f)$, is generated and shown as curve (c) in Figure 3-6. One can notice that some of the frequency

component magnitudes are negative. This is a direct indication that the amplitudes used in generating the exponentials $y_1'(t)$ and $y_2'(t)$ were larger than they should have been. Had $y_1'(t)$ and $y_2'(t)$ been exactly known (and f_1, f_2, exactly known), β_1, β_2 would be zero. Thus, $\ddot{Y}(f)$ is a measure of the error in estimating β_1, β_2 (and f_1, f_2). We can obtain a more accurate estimate of β_2 as: $\beta_2'' = \beta_2' - \left|\ddot{Y}(f = f_2')\right|$.

In this case $\left|\ddot{Y}(f = f_2')\right| = 0.086$ and thus $\beta_2'' = 0.746$, which we use to generate $y_2''(t) = 2\beta_2'' e^{-t \cdot f_2'}$. We generate a new $\dot{y}(t) = y(t) - y_2''(t)$ with corresponding frequency spectrum $\dot{Y}(f)$, shown as curve (b) in Figure 3-7.

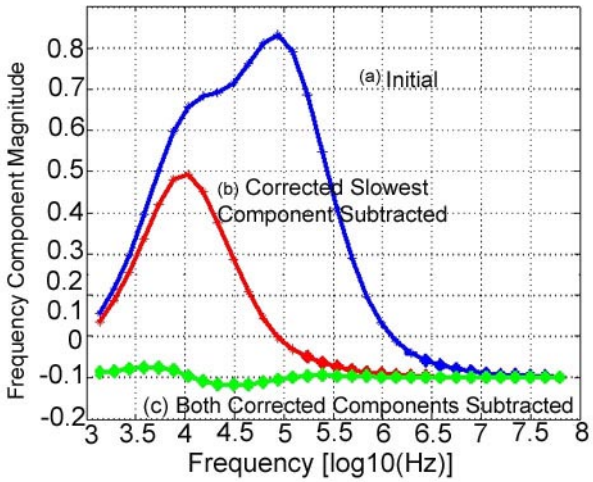


Figure 3-7
Frequency spectrum of $y(t)$, imaginary component.

$\dot{Y}(f)$ does not approach zero at $f = f_2'$. Finally, from the peak in curve (b) in Figure 3-7, we obtain a more accurate estimate of β_1, as $\beta_1'' = 0.492$.

For comparison with the earlier result in Figure 3-6, the "error" curve, $\ddot{Y}(f)$, is shown as curve (c) in Figure 3-7. $\ddot{Y}(f)$ is much smaller in amplitude than previously obtained, but is still not zero because β_1'', β_2'' (and f_1', f_2') are only estimates of β_1, β_2 (and f_1, f_2). The values of β_1'' and β_2'' are proportional (by a factor of 1/2) to the amplitudes of each exponential in the signal $y(t)$. In the context of determining the amount of one substance present in a mixture of two substances: $\frac{\beta_1''}{\beta_1'' + \beta_2''} \times 100$ represents the amount, as a percentage, of one substance in the mixture, while $\frac{\beta_2''}{\beta_1'' + \beta_2''} \times 100$ represents the amount, as a percentage, of the other substance in the mixture. In this example, $\frac{\beta_1''}{\beta_1'' + \beta_2''} \times 100 = 40.14\%$, which that is close enough to the exact value given by $\frac{\alpha_1}{\alpha_1 + \alpha_2} \times 100 = 40.00\%$.

The algorithm described only corrects peak amplitudes. Peak frequencies can be similarly corrected, but this is not necessary for oil detection.

3.2 PIER I (Preliminary Prototype) Design

3.2.1 PIER Sensor Electrodes

PIER applications require a flat form factor and minimal disturbance to the mud flow. For these purposes we have used coplanar electrodes separated by a guard border to collect leaked electric current. Electrodes were prepared from 50 μm thick copper foil and encapsulated between two Teflon sheets, specially processed by Fluoro-Plastics Inc., PA. We etched one side of the sodium ammonia material so that it could be bonded with epoxy resin. The structure of the electrodes is shown in Figure 3-8.

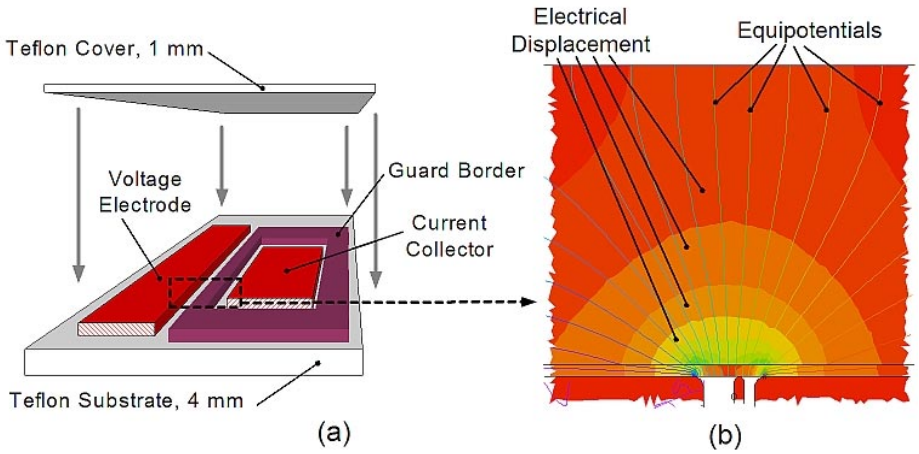


Figure 3-8
Structure of PIER sensor electrodes.
(a) design; (b) simulated distribution of electrical field.

For the laboratory test we have installed PIER sensor electrodes in the cover of a plastic chamber so we could change samples simply by moving this cover from one chamber with material to another. All chambers and the cover were laminated by adhesive aluminum tape for EM shielding (Figure 3-9).

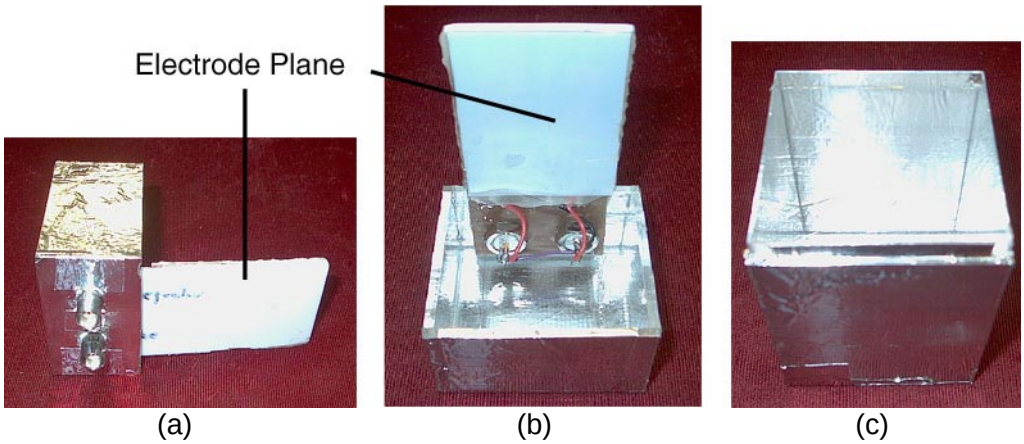


Figure 3-9
Sampler to test the PIER sensor.
(a) Sensor electrodes installed in the cover – external view;
(b) Same as (a) but internal view; (c) Sampler for the material.

The shielding of the electrodes prevents the stochastic electromagnetic fluctuations from influencing the data collected. The alternative, statistical filtration, is not desirable because we are interested in the detailed shape of each signal pulse.

3.2.2 Preliminary Analysis of PIER Sensor Head Analog Electronics

The PIER sensor head analog electronics consists of the generator of voltage pulses and the bi-channel integrator, the role of which is converting polarization currents in both parts of the PIER probe to their integrals, the electric charges. The principle of operation is shown in Figure 3-10.

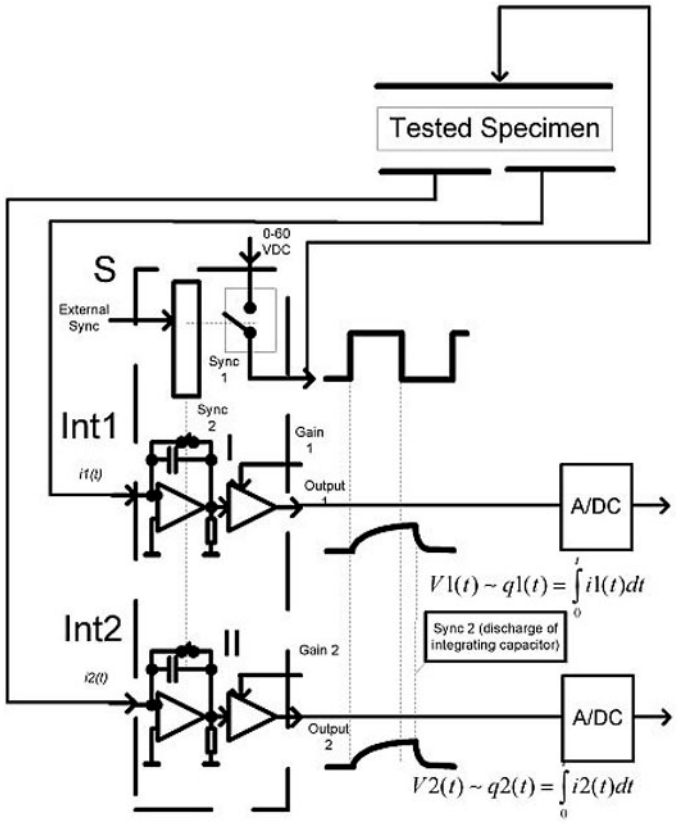


Figure 3-10
The principle of operation of the PIER sensor head analog electronics.
S = the switch generating the voltage pulses; Int1 and Int2 = integrating channels.

The integrator circuit accepts a pair of input currents from a capacitive probe with tested material. The input currents are polarization currents of dielectric. The probe has a pair of collecting electrodes separately connected to the inputs of the integrator circuit. The probe is charged through a common switch from an adjustable battery or power supply. The source voltage can vary from 5.5 to 60 V. Since the capacitance of the probe is 100 pF or less, the probe can be charged to 90% of the source voltage in <200 ms.

The integrator circuit comprises a pair of equal integrators: Integrator1 and Integrator2 (see Figure 3-11). Each integrator provides a voltage that can range from 10 mV to 10 V. The operation of Integrator1 (see Figure 3-11(b)) is further discussed, and Integrator2 (see Figure 3-11(c)) operates identically. A sync signal is applied to a Schmitt trigger to control operation of the integrator circuit. On the positive edge of the sync signal, a pair of switches in Integrator1 open to start the integration. Subsequently, the charging of the probe starts. The

delay is set by a delay network that drives another Schmitt trigger. This prevents oscillations of all switches even when the sync signal changes very slowly.

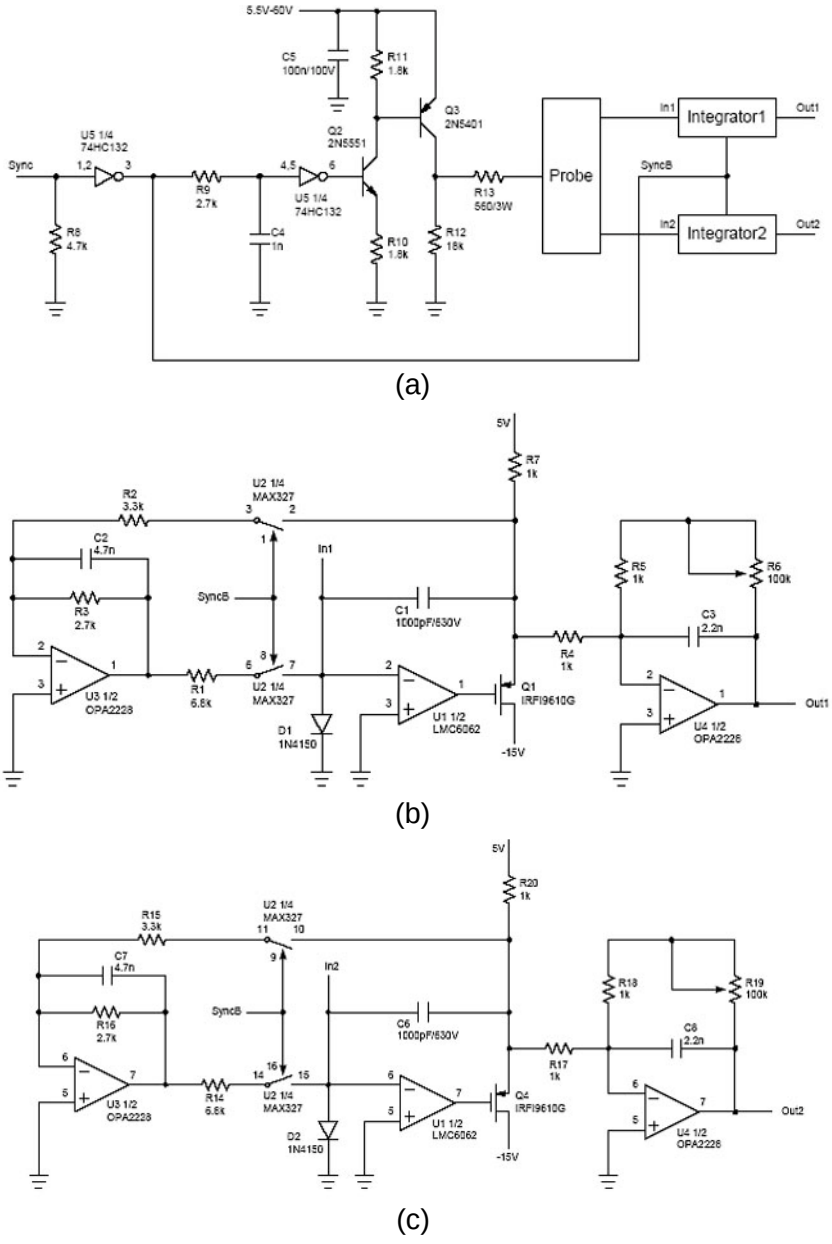


Figure 3-11
PIER sensor head analog electronics. (a) PIER sensor head analog electronics; (b) and (c) Integrator1 and Integrator2 respectively.

The probe is charged through a high voltage switch coupled in series with the supply source. The charging current is limited to 100 mA at 60 V through a resistor. The current limit is thus proportionally smaller at smaller source voltages.

The probe current is applied to the input of Integrator1, which is at virtual ground. Four components are connected to the input:

- An open switch
- A diode for protecting Integrator1 against excessive voltage
- An input of the integrating operational amplifier
- An integrating capacitor.

The accuracy of the integration is very high over a large portion of the integration time. Even if no current is applied to the input of Integrator1, its output voltage does not drop significantly over an extended period of time. To maximize accuracy, leakage currents of the input components are minimized in several ways:

- The open switch has inherently very low leakage current. This current is further reduced by maintaining zero voltage across the switch. Therefore, an operational amplifier driving the switch has very low offset voltage. Similarly, the potential of virtual ground at the input of Integrator1 is also very low.
- The input diode has very low leakage current due to the low potential of virtual ground at the input of Integrator1.
- The integrating amplifier has extremely low bias current and very low input offset voltage. This voltage determines the potential of virtual ground at the input of Integrator1.
- The integrating capacitor has very low leakage current. A high-voltage ceramic capacitor was chosen for this application.

The timing diagram for the PIER sensor analog electronics is shown in Figure 3-12.

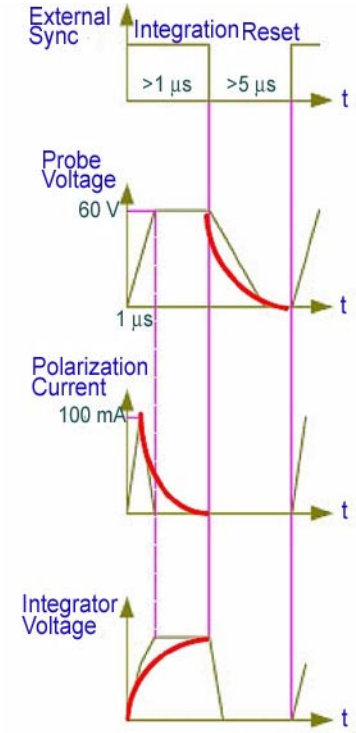


Figure 3-12
Timing diagram for PIER sensor head analog electronics.

Integrator1 is based on a conventional integrator that comprises an operational integrating amplifier and an integrating capacitor. Input current is applied to the inverting input of the operational amplifier. The integrating capacitor is connected between the inverting input and the

output of the operational amplifier. The noninverting input is grounded. At the beginning of the integration, the feedback capacitor is reset.

A large surge of input current would cause a voltage spike that could reach several volts at the input of Integrator1. Specifically, the capacitance of the probe and the integrating capacitor of the Integrator1 form a voltage divider. The capacitance of the probe can be as large as 100 pF. If the probe could be charged instantaneously, the input voltage would reach 60 V * 100 pF/ (1 nF + 100 pF) = 5.5 V. Furthermore, the integrating amplifier is incapable of responding to a narrow current surge of the input current.

A circuit protecting the input of Integrator1 is necessary. This is accomplished by connecting a diode across the input of Integrator1. It is also necessary to dramatically reduce the open-loop output impedance of the integrating amplifier, by using an output buffer. Without it, the current would flow through the output of the integrating amplifier and trigger its short circuit protection. This could heavily distort the integration due to effects associated with recovery of the amplifier.

Moreover, the buffer has to sustain the (relatively) large surge current of 100 mA that can flow at the very start of the integration. At 15 V supply voltage, the buffer would dissipate 1.5 W. Instead of an expensive power buffer, a MOSFET was chosen. The MOSFET operates as a voltage follower, and is significantly faster than the integrating amplifier.

On the negative edge of the sync signal, the pair of switches in Integrator1 closes to reset the integrating capacitor. Subsequently, the discharging of the probe starts. After a delay, the switch in series with the probe opens. The probe is discharged through a resistor connected in parallel with the probe. A small current of reverse polarity is applied to the input of Integrator1. The output voltage of the integrating amplifier is applied through one switch to another amplifier. The output voltage of the latter amplifier is applied through the other switch and a series resistor to the input of Integrator1. The current flowing through the resistor is thus negative and discharges the integrating capacitor. At the end of the reset, voltages across both switches are zero. Then the integrator circuit is ready for another cycle.

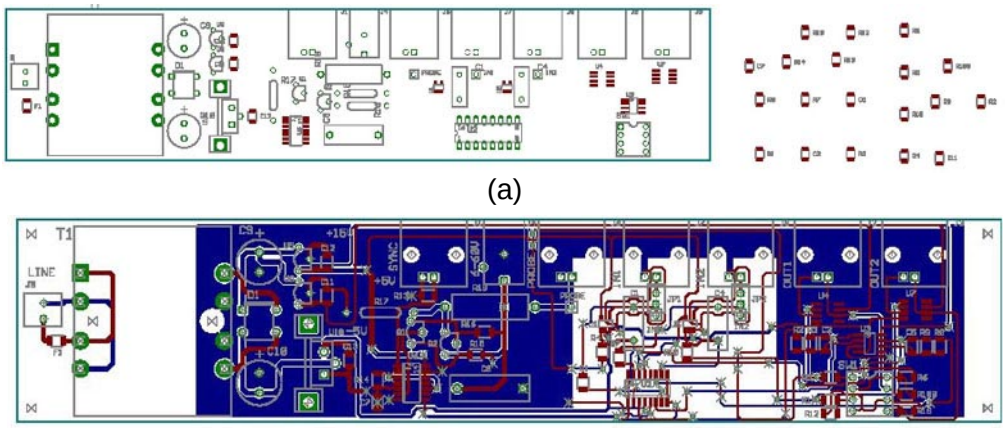
An output amplifier is used to amplify the output voltage of the integrating amplifier. The gain of the output amplifier is set manually in a range from -1 to -100. A positive input current from the probe results in a negative voltage at the output of the integrating amplifier. This voltage is thus amplified and inverted to produce a positive output voltage of Integrator1.

3.2.3 PIER Sensor Head Analog Electronics Printed Circuit Layout and Board Fabrication

The schematics presented in Figure 3-11 were transferred to the design of the printed circuit board (PCB). The disposition of PCB elements and tracing are presented in Figure 3-13.

These PCBs were fabricated, assembled with electronic devices, and tested. Figure 3-14 presents the assembled PCB with installed electronic components and BNC connectors (will be not used in the final assembly) for testing. We also installed a specialized power supply on the PCB solely for laboratory testing. This power supply imitates the battery power with short links to the sensor electronics, which eliminates several problems with electromagnetic influences on conventional laboratory power supplies. This power supply also can be used in conventional ground applications with power from the AC power network.

During the testing of the assembled PIER sensor head analog electronics we investigated problems with overload of operational amplifiers and also with overvoltage at FET inputs of these amplifiers. These problems were solved, and the modified schematics of the PIER sensor head analog electronics are described in the following sections.



(a)

(b)

Figure 3-13
PCB for PIER sensor head analog electronics:
(a) position of elements, and (b) PCB layout with tracing.

Figure 3-14
Assembled PCB of PIER sensor head analog electronics.

3.2.4 Modified Integrating Circuit Operation

We modified the initial design (see Figure 3-11) based on test results. Figures 3-15, 3-16, and 3-17 present designs for the probe driver (pulse generator and synchronizing circuits), integrator, and power supply, respectively.

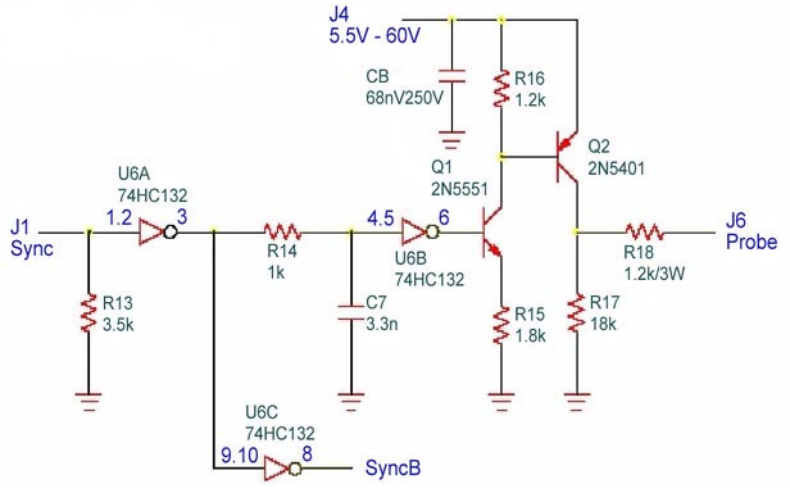


Figure 3-15
Voltage and synchronizing pulse generation circuit (probe driver).

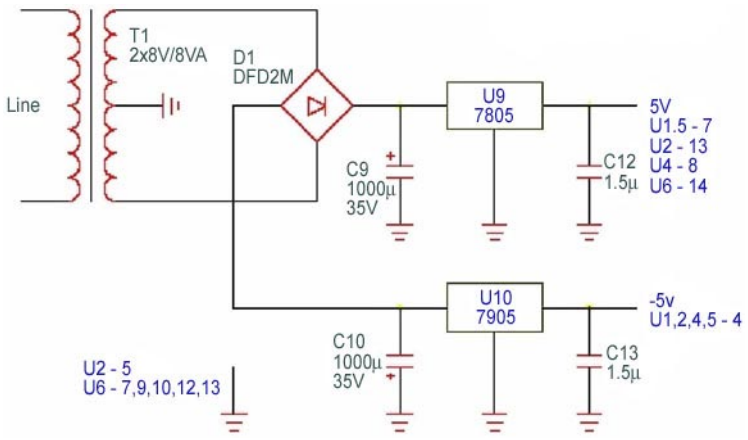


Figure 3-16
Power supply (only in PIER I).

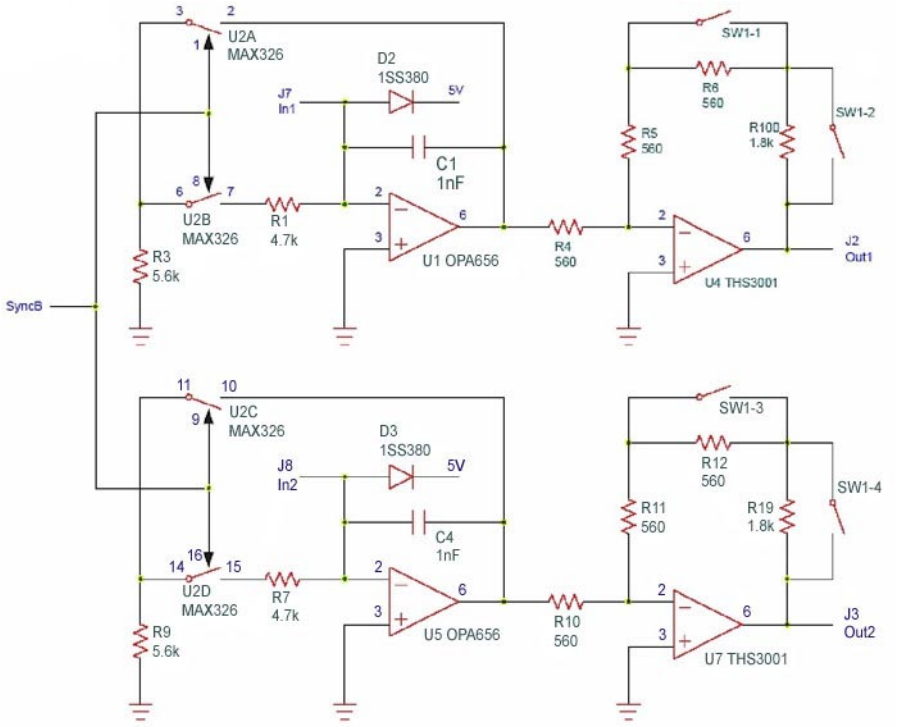


Figure 3-17
Integrator.

Below we analyze details of the PIER sensor head operation with references to Figure 3-17. The integrator circuit comprises a pair of identical integrators. The sync signal controls operation of both integrators. Therefore, the operation of only one integrator is discussed further.

One of the probe currents is applied to the input of the integrator. The input is connected to the inverting input of operational amplifier U1, the anode of diode D2, resistor R1, and integrating capacitor C1. The noninverting input of U1 is grounded.

The integrating amplifier has very high accuracy, in particular, an extremely low bias current of 2 pA. This is essential for maintaining high accuracy when the integration extends over a long

period of time. Moreover, the integrating amplifier has a low offset of 250 nV, high output current capability of 70 mA, and high slew rate of 290 V/μs.

The offset voltage determines the potential of virtual ground at the input of the integrator. The output current capability exceeds 50 mA, which is required to charge the probe. The slew rate of the integrating amplifier also exceeds the required rate. C1 is charged at a rate having a peak of 50 mA/1000 pF = 50 V/μs regardless of the capacitance of the probe. The peak is proportionally smaller at lower source voltages. Moreover, the rate is logarithmic and drops quickly during charging.

D2 protects the input of the integrator under abnormal operating conditions. For example, the electrodes of the probe can be accidentally shorted, which may result in a peak current of 50 mA being applied to the input of the integrator for an extended period of time. D2 has the cathode connected to the power supply rather than the ground. By reversely biasing D2, its junction capacitance is cut to 2 pF. If the integrator voltage exceeds the supply voltage of U1, a portion of the integrator input current flows through the internal diode of U1. The peak current of the internal diode is 30 mA, wherein the diode has a relatively large forward voltage.

The cathode of D2 can be alternatively grounded; the main advantage is reduced leakage current. Furthermore, the excessive input current is injected into the ground. D2 provides the proper protection even if the supply current is below 50 mA. D2 can employ two or more diodes connected in series as yet another alternative. The junction capacitance is at least cut in half without increasing the leakage current. R1 isolates the integrator input from the output capacitance of switch U2B. C1 is a plastic film capacitor whose insulation resistance is about 500 Tohms.

The output amplifier U4 is a current feedback amplifier with a slew rate of 6500 V/μs. U4 has the gain set manually to -1, -2, -4.2, or -5.2. U4 can be supplied from +15 V and thus deliver output voltages above 10 V. However, the positive supply voltage is presently +5 V. The gain setting resistors are relatively small in order to produce high bandwidth. A higher supply voltage could cause U4 to overheat.

The sync signal is set to high in order to start the integration. Switches U2A and U2B are open, and both are grounded through resistor R3. The voltage across U2A is equal to the output voltage of U1. The voltage across U2B is near zero, as the other end of U2B is at ground potential.

The sync signal is applied to inverter U6A with Schmitt input. A high-voltage switch, Q2, applies the source voltage to the probe after a delay of several microseconds. The delay is set by the network R14 and C7, which controls another Schmitt inverter, U6B. U6B drives a high-voltage current source, transistor Q1. This limits the base current of the following Q2.

The probe is charged through R18. The source voltage can vary from 5.5 V to 60 V. The peak current of Q2 is limited to 50 mA at 60 V. If the capacitance of the probe is 100 pF, the probe will be charged to 90% of the source voltage in less than 360 ns regardless of the source voltage.

The sync signal is set to low to reset the integrator circuit. U2A and U2B apply the output voltage of U1 to the integrator input. The output voltage is actually slightly higher due to the on-resistance of U2A. The output voltage of U1 is near zero, and C1 is discharged.

Q2 opens after several microseconds. R14 and C7 determine the delay again. The probe is discharged through series-coupled resistors R17 and R18. The sum of the resistor values is

16 times larger than the value of R18. The current discharging the probe is applied to the input of the integrator and has reverse polarity. However, the current is 16 times smaller than the peak charging current. The protection against excessive negative voltage at the integrator input is unnecessary.

The modified PCB was fabricated (see Figure 3-18) and we have installed components and mounted the device in the shielding case (see Figure 3-19).

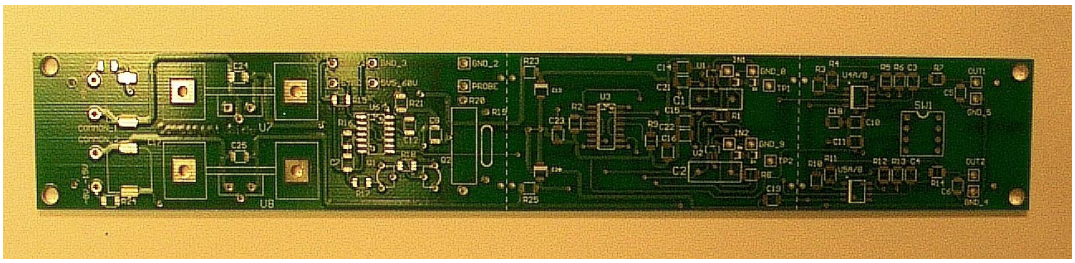


Figure 3-18
Modified printed circuit board (PCB) of PIER I.

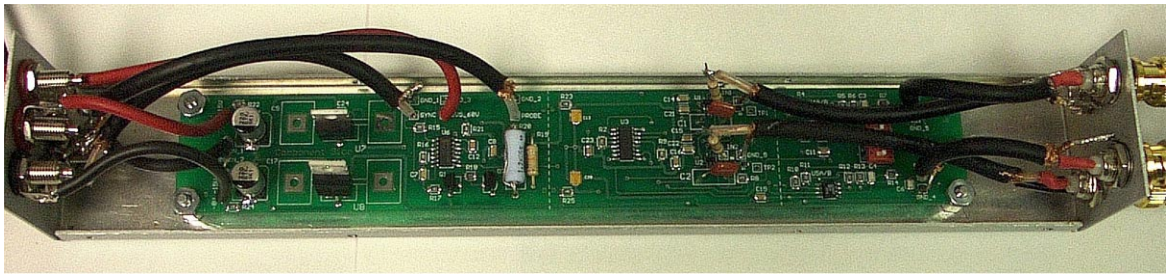
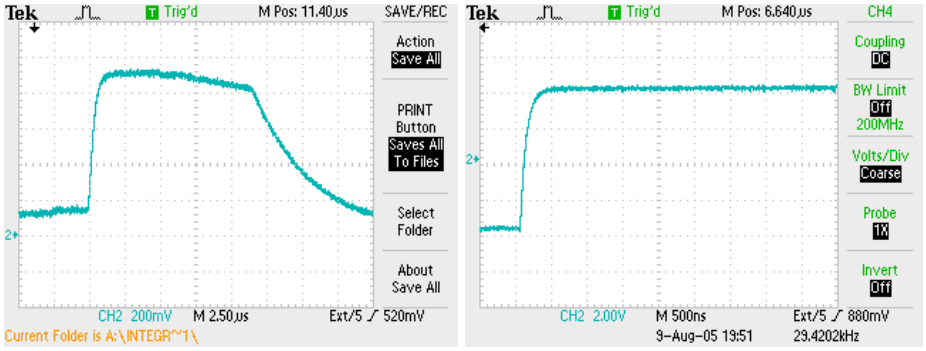


Figure 3-19
PIER I PCB installed in the shielding case.

3.2.5 Tuning of the PIER I PCB

In the initial tests, the PIER PCB integration time was excessive due to the limiting resistor at the output of the probe driver. This is illustrated in Figure 3-20, where the output signal for the mud-loaded input is shown for the initial (with resistor) configuration (Figure 3-20(a)) and without this resistor (Figure 3-20(b)).



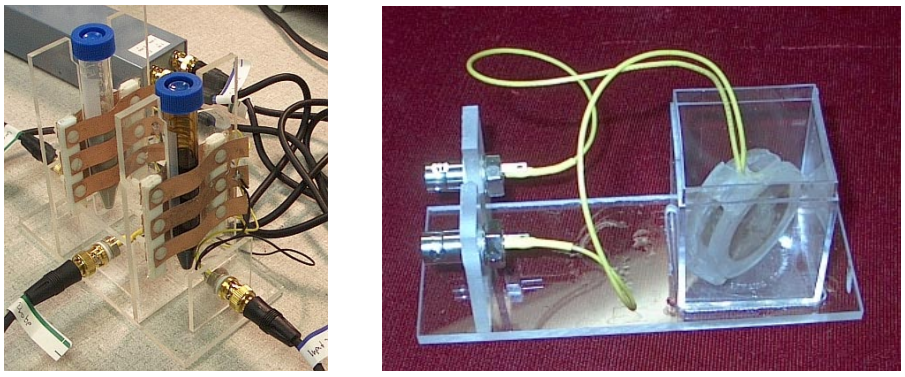
(a) (b)

Figure 3-20
The output pulse shape (a) with a limiting resistor and (b) without one.
Note the different time scale — 2.5 µs at (a) and 500 ns at (b).

The slow discharge of the integrating capacitor can be seen in Figure 3-20(a), caused by leakage along the PCB surface (the problem was solved by cleaning the board with FC-77 electronics solvent from 3M). Thus the design of the PIER II final prototype included the careful isolation of the integrating op-amp.

3.2.6 Test of Primary PIER I Prototype

We fabricated several electrode systems for testing the PIER prototype with mud, oil, and mixtures. At first we kept the fluids in plastic probes so when we replaced the test material we did not have to clean the probe electrodes. Such electrodes are shown in Figure 3-21(a). However, the weak sensitivity and influence of the plastic wall (polypropylene) required us to change to brass electrodes with a ferroelectric layer as an insulator (we have used the piezoelectric structure of a simple speaker).



(a) (b)

Figure 3-21
Test electrodes: (a) external through the polypropylene wall;
(b) dipped into the material, with ferroelectric insulation.

The PIER core electronics prototype was tested in a laboratory setup with power from commercial power supplies and signal recording by oscilloscopes. The setup is shown in Figure 3-22.

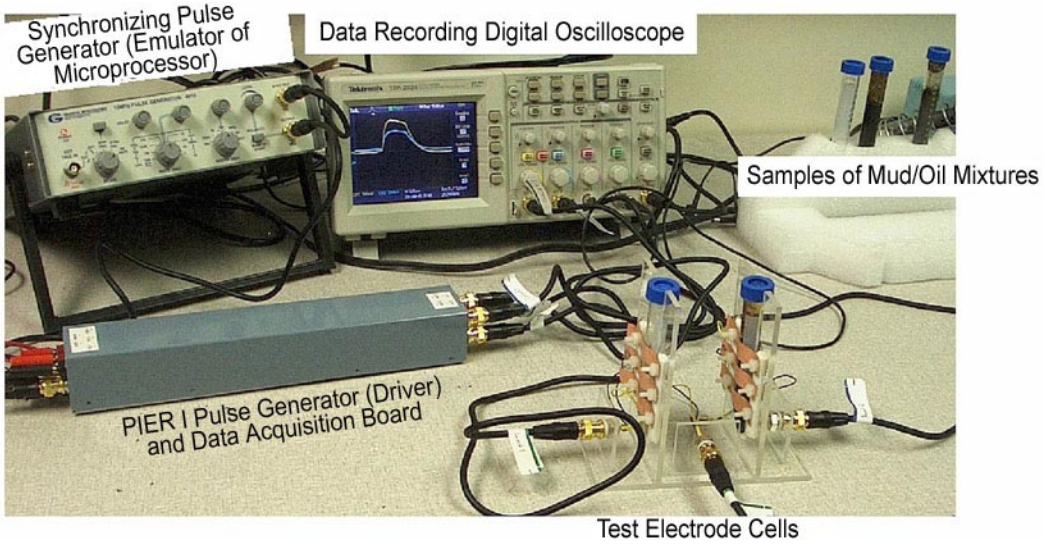


Figure 3-22
Test setup for the PIER I prototype.

The PIER I prototype was tested with three kinds of materials — pure mud, pure oil, and a 50/50 mix of mud and oil. The output signals obtained (polarization charge vs. time) are shown in Figure 3-23.

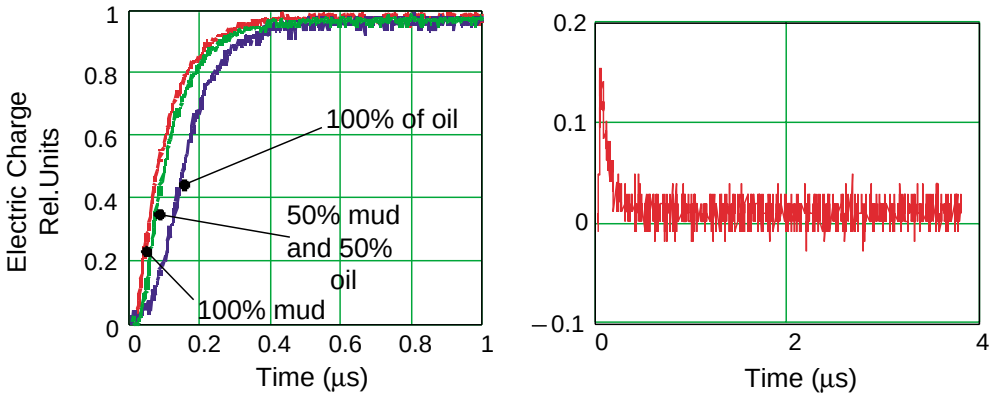


Figure 3-23
Output signal of tested PIER I prototype: (a) Shape of time-domain response to the step-like application of voltage to various materials; (b) difference between material 1 and material 2.

Recorded time-domain data were processed in MathCAD 2001 by Fast Fourier Transform (FFT). The algorithm of data processing included the normalization of the time scale and elimination of the permanent offset with following FFT. Normalized data are presented in Figure 3-24 and the spectra of effective dielectric permittivity are shown in Figure 3-25. A clean difference is observed in the polarization rate between the mud and oil, while the mixture shows very little difference from the mud.

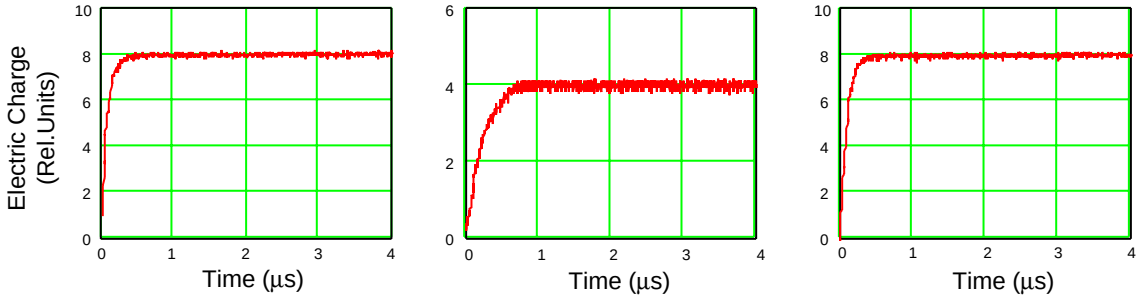


Figure 3-24
Increasing of polarization charge on the (a) mud, (b) oil and (c) 50/50 mixture of mud and oil. The difference in the polarization rate between mud and oil is easily observable.

Among these three materials, the lowest losses occur in the mud (due to its good conductivity) and the greatest losses occur in the mixture because of interfacial polarization at boundaries of oil microdroplets. The position and amplitude of the peak in loss spectra are the basis of the measurement of the fluid composition. The plot in Figure 3-26 compares these spectra.

The frequency shift between oil and mud is clear. At the same time, the mixture peak corresponds to the mud peak because conductivity occurs at the oil droplet surface due to the conductivity of mud. Therefore the variations of the peak amplitude mean oil is penetrating the hole, and the shift of the peak to lower frequencies means oil is filling the downhole.

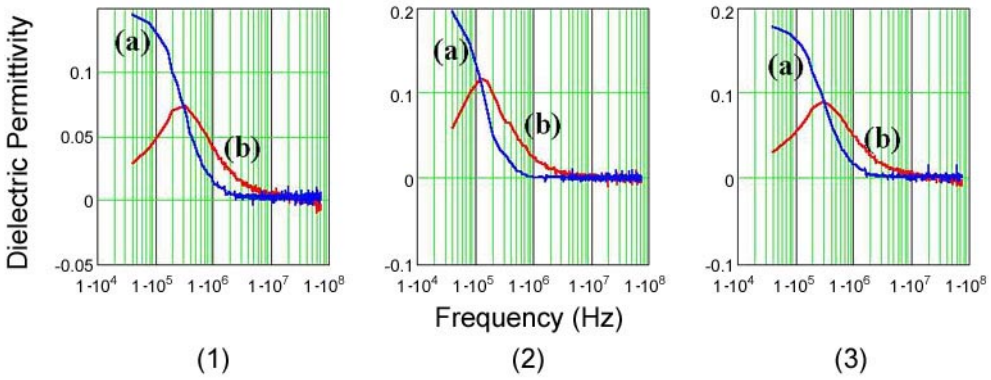


Figure 3-25
Effective spectra of dielectric permittivity for (1) mud, (2) 50/50 mixture of mud and oil, and (3) oil. (a) and (b) are real (dielectric constant) and imaginary (dielectric loss) parts of dielectric permittivity.

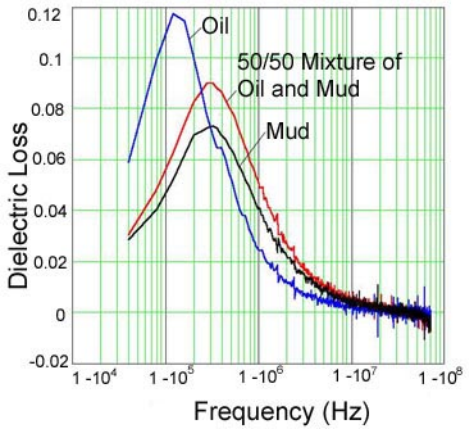


Figure 3-26
Spectra of dielectric loss.

3.2.7 Data Acquisition and Processing Controller (Preliminary Prototyping)

The data acquisition and processing controller (later, signal processor) controls sensor operation by initiating a pulsed voltage and resetting integrators, digitizes the analog output of integrators, and performs signal processing. The purpose of the signal processor is to convert an analog signal into digital form and then perform a Fast Fourier transform on the digitized samples. The block diagram of the PIER data acquisition and processing unit is shown in Figure 3-27.

The signal processor contains the following integrated circuits (ICs), which work synchronously:

- Input buffer
- Single ended differential amplifier
- Analog-to-digital converter (12 bit @ 10 Msp)
- Programmable clock oscillator × 2
- FIFO (first in, first out, with 32 kb of buffer memory)
- FIFO timing control circuitry that includes:
  - Inverter buffer
  - Multiplexer
  - Microcontroller.

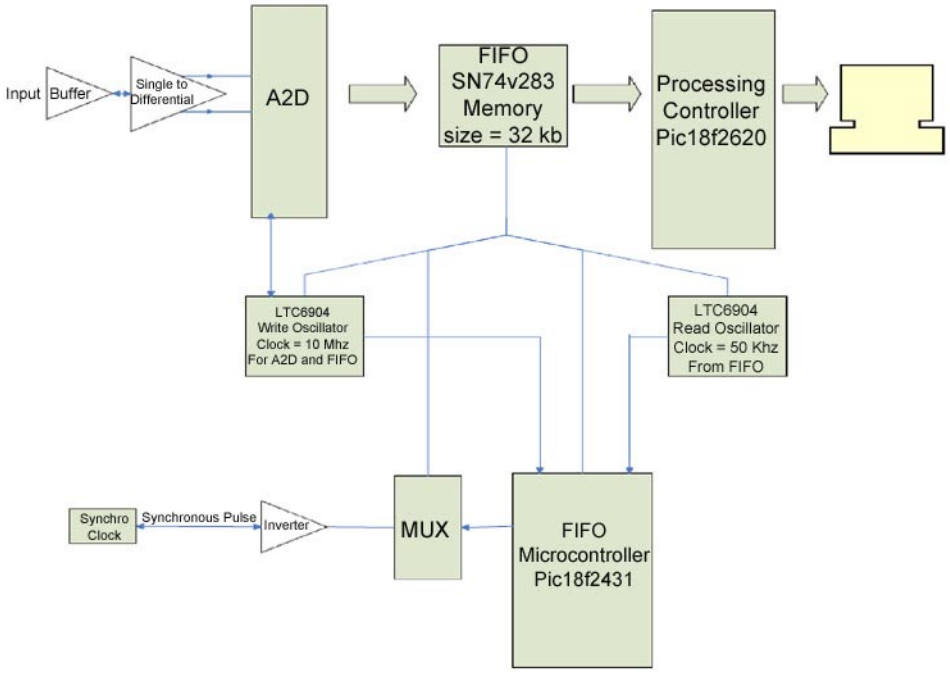


Figure 3-27
PIER data acquisition and processing unit. The peach element in the right upper corner is the interface with the data transmitter (for example, the MWD tool from Schlumberger).

3.2.7.1 Analog Signal Digitizer

The analog input signal goes through the input terminal, where it is buffered and transformed from a single-ended 5 V signal input into a differential signal with a maximum swing of 2 Vpp (peak-to-peak). The differential signal is fed into the analog-to-digital converter (ADC) (see Figures 3-28 and 3-29). This converter, with 12 bits of digital output, can process data at 12 million samples per second. However, the microcontroller can only read the data at 50 thousand two-byte samples per second. To override this bottleneck, we have implemented the FIFO buffering memory, taking 32 kbit chunks of data, which is the capacity of the FIFO memory. These chunks are taken from different pulses with timing shifts described below.

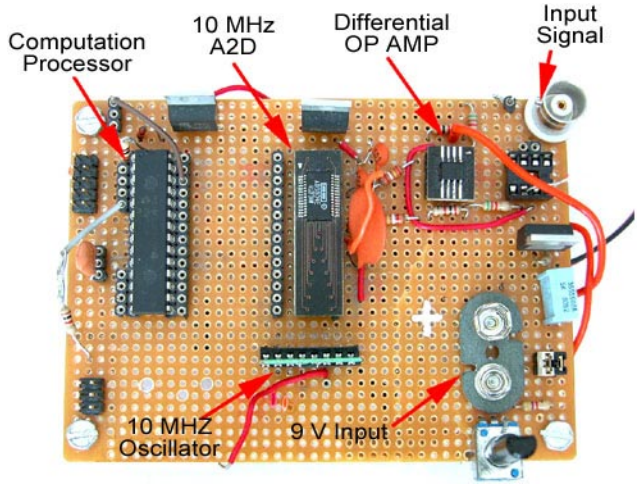


Figure 3-28
Analog-to-digital converter and the processing controller board.

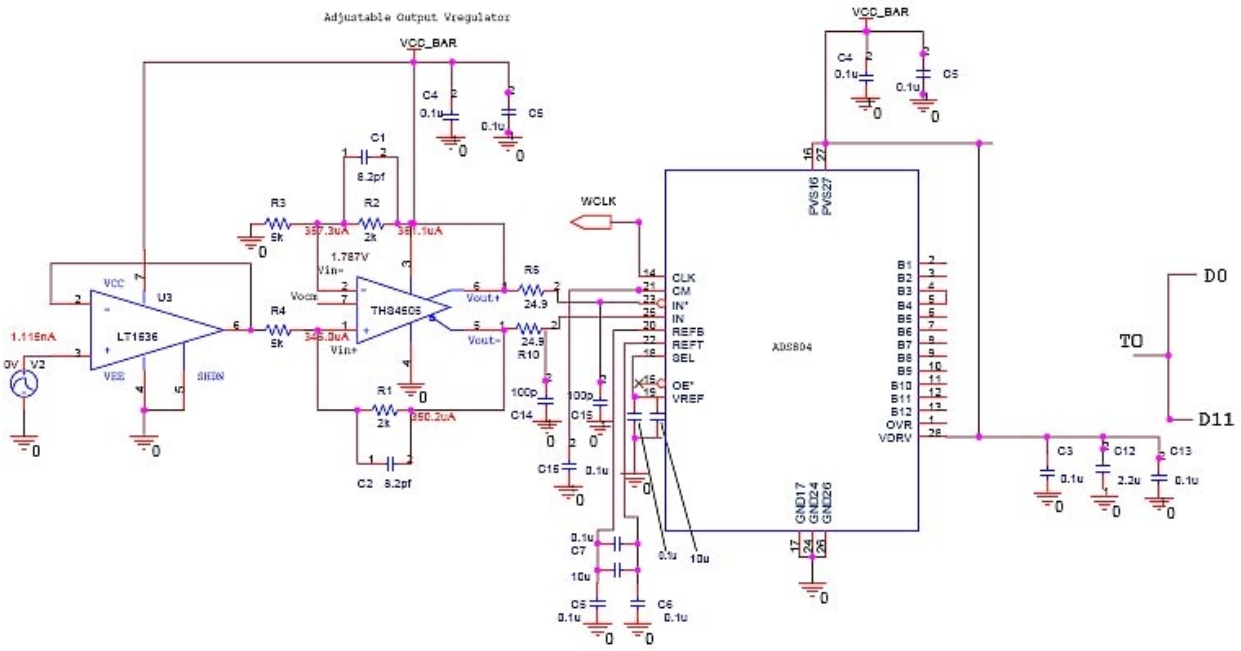


Figure 3-29
Digitizer scheme.

After the analog input is digitized, the signal goes through the FIFO chip that serves as the data buffer. The FIFO saves the digitized signal in chunks of 30 μs at a rate of 10 mega samples per second. After saving 30 μs worth of data, the FIFO control circuitry disables the FIFO data saving and transfers the data to the computation processor at a rate of 50 kHz. Once the microcontroller finishes saving the data, the FIFO empty flag signals that the FIFO is empty, and the process is repeated.

Each following data chunk is acquired at an interval of one pulse period plus 30 μs. Thus data are acquired continuously from different pulses of polarization as presented in Figure 3-30.

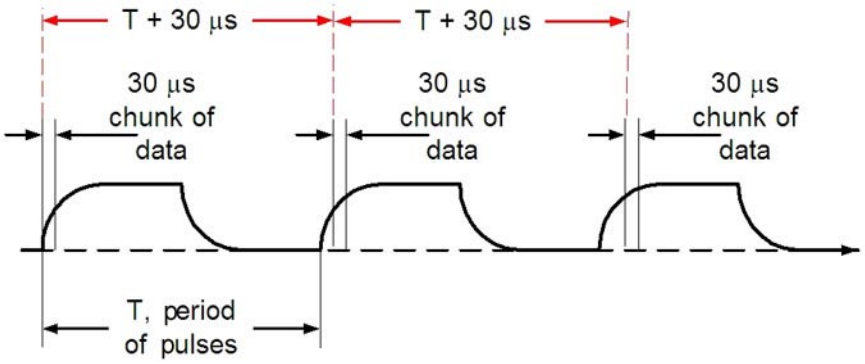


Figure 3-30
Consecutive data acquisition cycles by buffering 30 μs data chunks.

The implementation of consecutive data extraction cycles overcomes the bottleneck in transferring data from the ADC to the central processor memory. The FIFO circuit with data input and output terminals is shown in Figures 3-31 and 3-32. The consecutive data acquisition

is controlled by the synchronization circuit (see Figure 3-27) under the direction of the central processor. The synchronization circuit produces a square wave signal with an amplitude of 5 V.

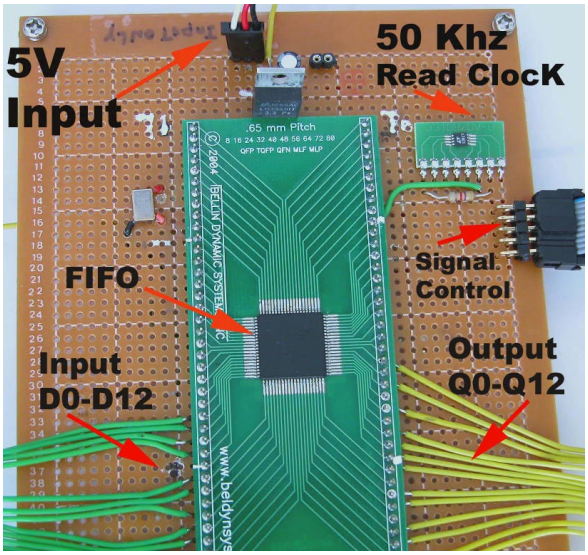


Figure 3-31
FIFO circuit (breadboard test before fabrication of PCB).

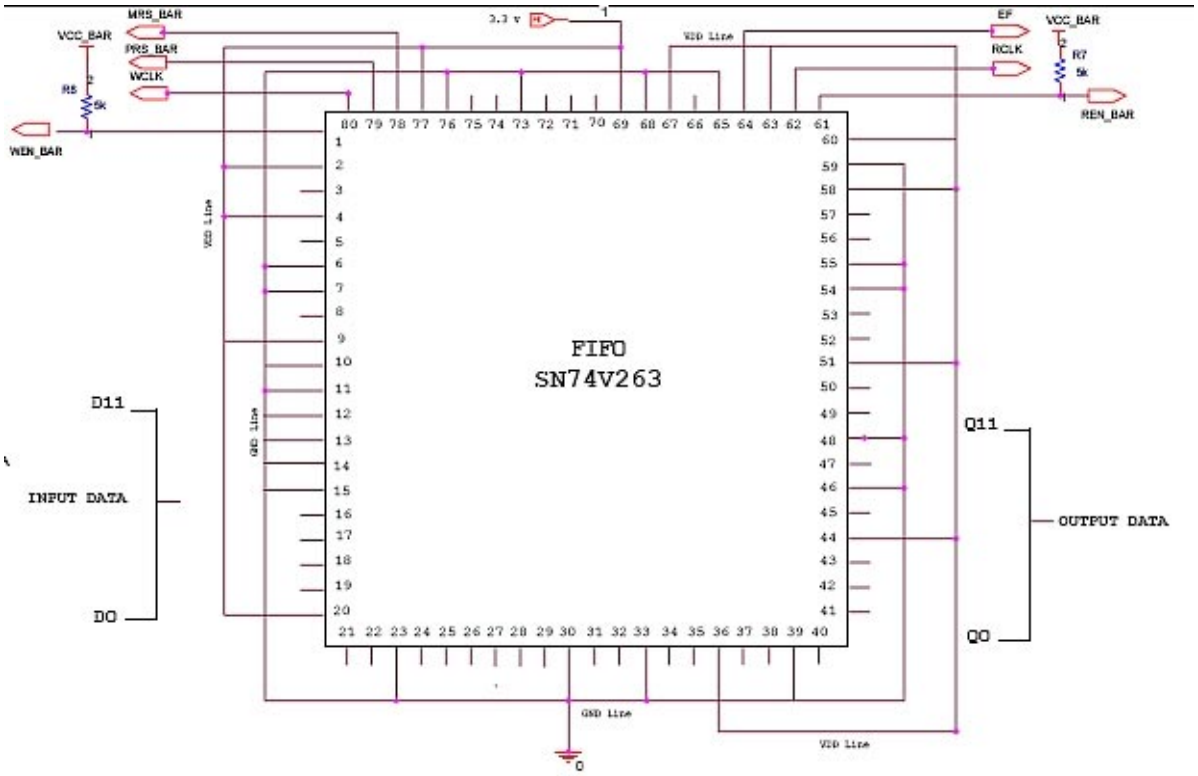


Figure 3-32
Design of FIFO connections.

3.2.7.2 FIFO Control Circuitry

The FIFO control circuitry supports the major function of data acquisition in PIER. It controls all the timing of input and output signals going to the FIFO and out to the computation processor. This circuit is presented in Figures 3-33 and 3-34.

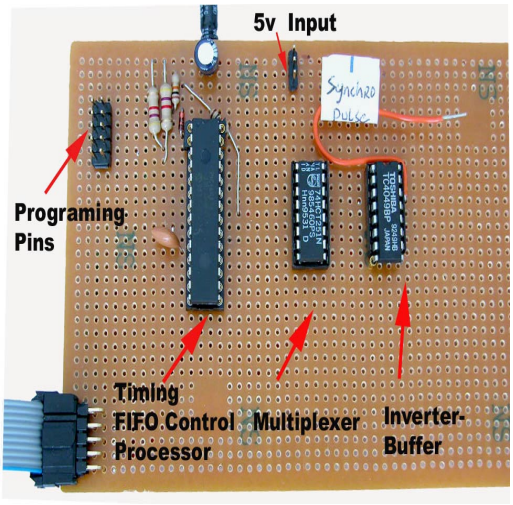


Figure 3-33
FIFO control circuitry (breadboard test before fabrication of PCB).

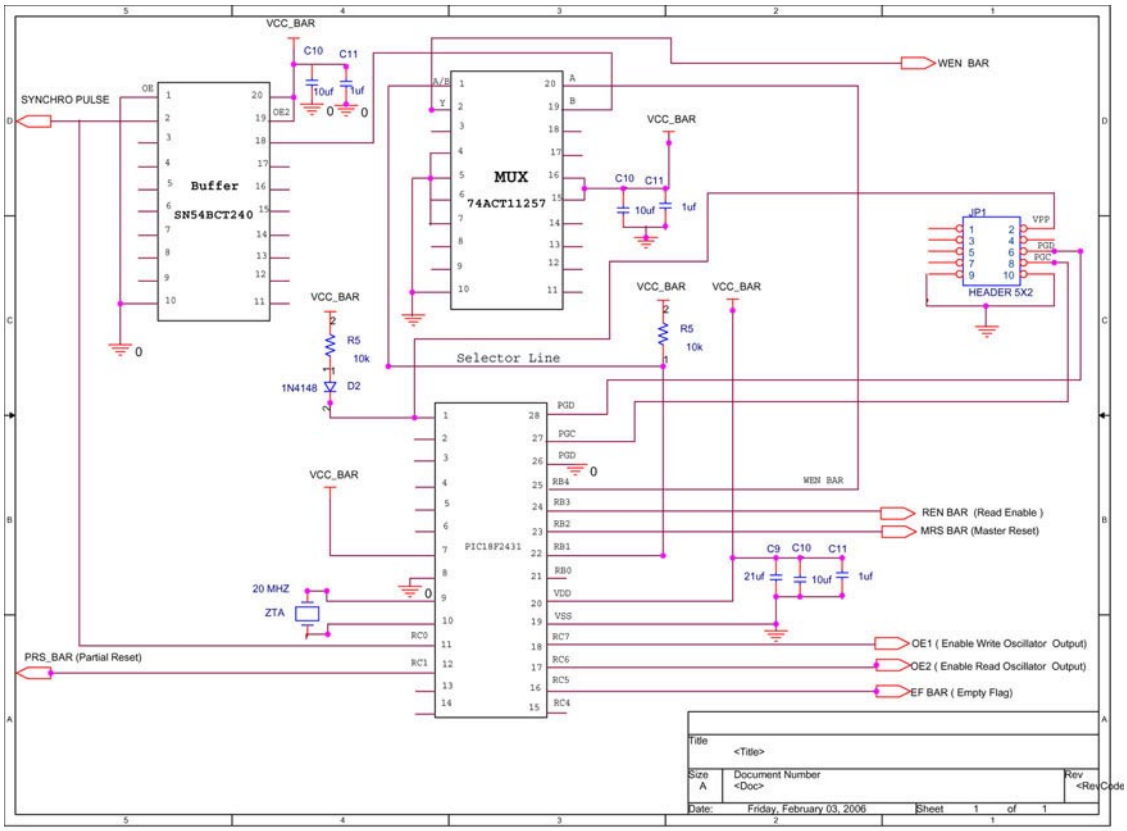


Figure 3-34
Design of FIFO control circuitry.

The FIFO control circuitry signals tell the FIFO when to start and stop sampling, and when to transfer the stored data to the central processor. It uses the commands:

- WEN BAR: Enable write to the FIFO
- REN BAR: Enable read operation from the FIFO
- WCLK: Write clock
- RCLK: Read clock
- MRS BAR: Master reset
- PRS BAR: Partial reset
- EF BAR: Empty flag.

For the FIFO to function properly, the minimum timing requirements must be met. Initially, the FIFO must perform master reset (MRS BAR). The master reset signal level must be low, while read enable (REN BAR) or write enable (WEN BAR) signals are held high. Once reset, the read enable signal is held high for 30 μs and then disabled (low level). The write enable regime is then enabled until the central processor reads all the data and the FIFO empty flag (EF BAR) signal is low. After all data are transferred to the central processor and the FIFO empty flag is raised to the high TTL level, the system waits for the next synchronous pulse, and this operation repeats. The timing of the FIFO control circuit is supported by two system oscillators, shown in Figure 3-35.

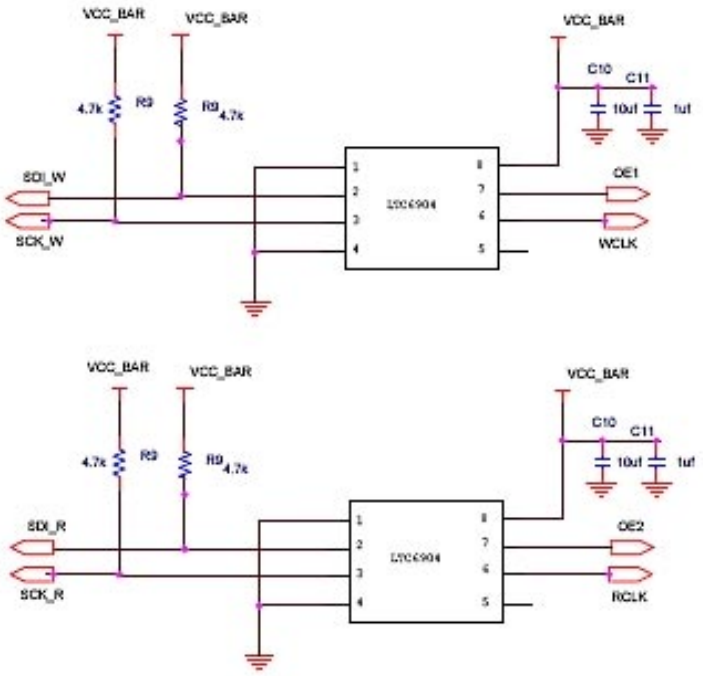


Figure 3-35
System oscillators.

3.2.8 Implementation of a Compact Algorithm of the Fast Fourier Transform

In Section 3.1.2 we showed that a characteristic of dielectric spectrometry is the continuous rise of the transmitted charge. Because the rate of rise continuously decreases, data can be approximated linearly in the time domain with sequentially increased time intervals between the selected data. Thus the charge vs. time function can be linearly approximated at each of these intervals as

$$q(t)_k^{k+1} = \frac{q_{k+1}}{t_{k+1} - t_k}(t - t_k) + q_k \quad , \tag{3-19}$$

where q_k and q_{k+1} are measured at moments t_k and t_{k+1}. The purpose of this approximation is for the operation with data in a logarithmic scale with an irrational base, for example, a square root of 2, which does not match the permanent data acquisition rate. The advantage of a logarithmic scale is the reduction of data processed. For example, 1024 measurements will be reduced to 10 with a logarithmic base 2 or to 20 at the base $\sqrt{2}$.

The targeting function is the imaginary part of a complex admittance between probe electrodes that is proportional to the complex dielectric permittivity. We have demonstrated that the frequency dependence of this parameter is the Fourier transform of the electric current in the time domain. Therefore moving to the polarization charge, $q(t)$, (integral of the current, $i(t)$) leads to the next formula according to the differentiation theorem for the Fourier transform

$$e^*(w) = F\{i(t)\}_w = jwF\{q(t)\}_w = jw\int_0^\infty q(t)e^{-jwt}dt \quad . \tag{3-20}$$

Eq. (3-19) enables conversion of the full range integral Eq. (3-20) to the sum of partial integrals

$$e^*(ww) = jw\sum_{k=0}^{n-1^t}\int_{t_k}^{k+1} q(t)e^{-jwt}dt = jw\sum_{k=0}^{n-1} y_k \quad , \tag{3-21}$$

where the partial integral y_k can be presented, by Eq. (3-19), as

$$y_k = -\frac{1}{jw}(q_{k+1}e^{k+1} - q_k e^{-jwt_k} + \frac{q_{k+1} - q_k}{t_{k+1} - t_k}\frac{e^{-jwt_{k+1}} - e^{-jwt_k}}{jw}. \tag{3-22}$$

When y_k in the form of Eq. (3-22) is inserted in the sum of Eq. (3-21), the first two exponential members in brackets reciprocally go away because each $q_{k+1}e^{-jwt_{k+1}}$ in the y_k has negative $q_k e^{-jwt_k}$ in the next y_{k+1}. There are two members left - $-q_0 e^{-jwt_0}$ because q_0 = 0 and $q_\infty e^{-jwt_\infty} \to 0$ because $e^{-\infty} \to 0$ while q_∞ is the limited value. Thus the final form of dielectric permittivity is

$$\varepsilon^*(w) = \frac{1}{jw}\sum_{k=0}^{n-1}\frac{q_{k+1} - q_k}{t_{k+1} - t_k}(e^{-jwt_{k+1}} - e^{-jwt_k}) \quad , \tag{3-23}$$

of which the imaginary part is

$$\mathrm{Im}[e^*(w)] = \frac{-1}{w}\sum_{k=-}^{n-1}\frac{q_{k+1} - q_k}{t_{k+1} - t_k}(\cos wt_{k+1} - \cos wt_k) \quad . \tag{3-24}$$

All t_k are defined by the minimal time interval between data acquired, t_0, as $t_k = t_0 B^k$, where B is the base of the logarithmic time scale.

To test the spectral resolution of the algorithm described, we have simulated the input signal as the sum of two exponents in MathCAD (see Table 3-1).

Table 3-1. Simulation Program for MathCAD 2001

Simulation of the PIER algorithm by M. Reznikov

$n := 70$ number of data

$i := 0 .. n$ time index

$j := 0 .. n$ frequency index

$t0 := 10^{-7}$ minimal time

$b := \sqrt{2}$ constant of logarithmic increment

$t_i := t0 \cdot b^i$ time variable

$w_j := \frac{(2 \cdot \pi)}{t0 \cdot b^j}$ frequency variable

$\tau 1 := 10^{-4}$ $\tau 2 := 10^{-2}$ model time constant

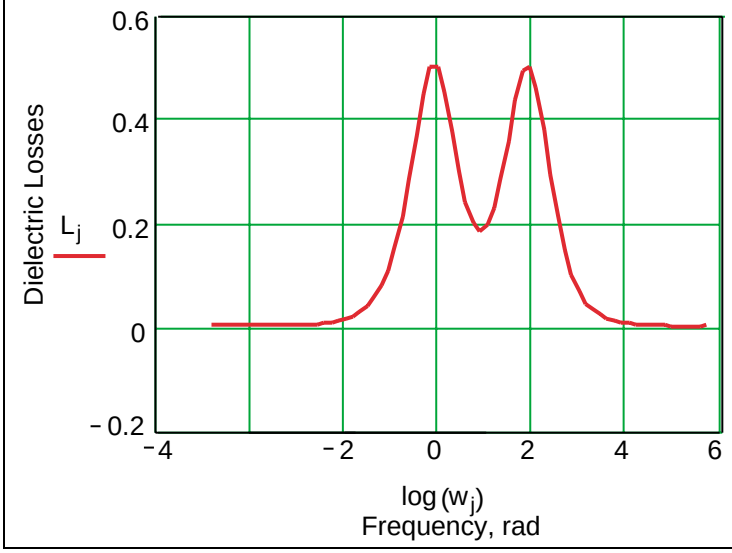
$a1 := 1$ $a2 := 1$ amplitudes

$c := a1 + a2$

$q_i := c - a1\, e^{\frac{-t_i}{\tau 1}} - a2\, e^{\frac{-t_i}{\tau 2}}$ model function

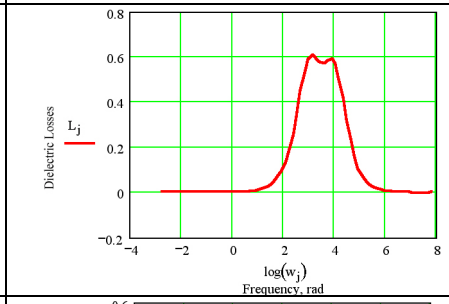
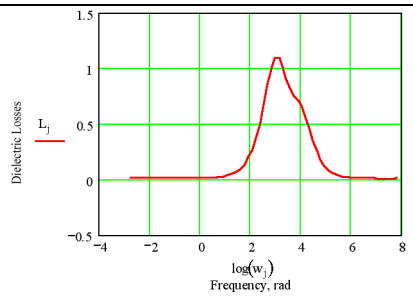
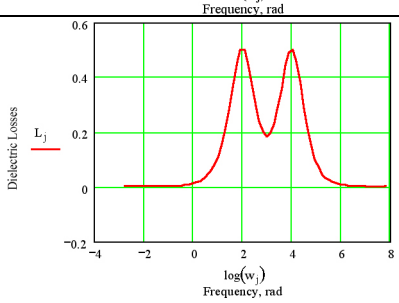
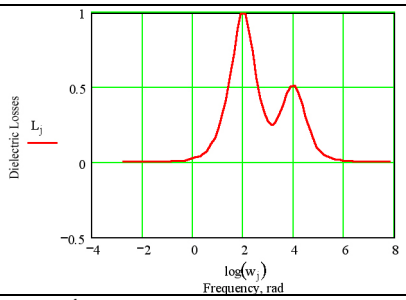
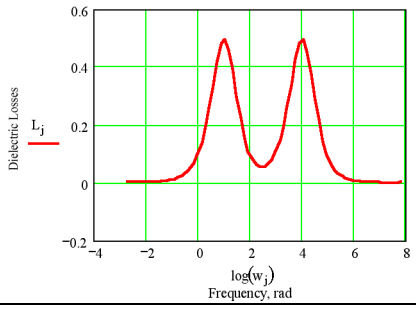
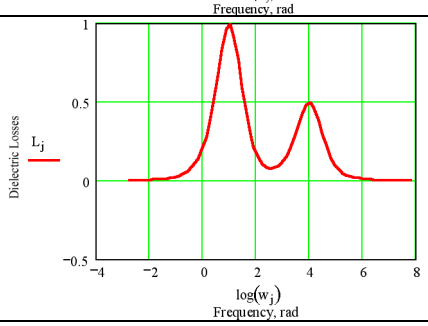
$$L_j := \frac{\sum_{i=0}^{N-1} (q_i - q_{i+1}) \frac{(\cos(w_j \cdot t_{i+1}) - \cos(w_j \cdot t_i))}{t_{i+1} - t_i}}{w_j}$$

output - losses



The example in Table 3-1 represents the case when time constants differ by 100 times, and both have the same amplitude. Table 3-2 presents simulation results at time constants $\tau 1$ and $\tau 2$, and amplitudes $a1$ and $a2$.

Table 3-2. Resolution of Two Relaxation Processes at Different Amplitudes and Time Constants

	$a1 = a2$	$a1 = 2a2$
$\tau 2 = 10\tau 1$		
$\tau 2 = 100\tau 1$		
$\tau 2 = 1000\tau 1$		

These plots demonstrate that peaks in the dielectric loss spectra cannot be resolved if relaxation times differ by less than 10 times. This is the natural physical limitation due to the wide, nonresonant nature of the dielectric losses. Thus we can conclude that high spectral resolution, i.e., a high density of calculated frequencies, is useless for dielectric spectroscopy, and logarithmic scaling with a base $\sqrt{2}$ (i.e., 6 points per degree of ten) is enough information.

3.2.9 Test of the PIER I System

3.2.9.1 Test System

To test the data acquisition and data processing algorithms, we used the virtual instrument (VI) emulation from NI LabVIEW 7. For digitizing and transferring the acquired sensor data onto a computer, we utilized data acquisition (DAQ) board PMD-1208FS from Measurement Computing. This USB DAQ module contains eight channels of 12-bit analog input with a maximum sampling frequency of 50 KS/s. The advantage of having eight channels is that it would allow us to acquire eight analog signals in parallel; however, the sampling frequency would also have to be divided by this number of channels. Thus, in order to maximize our sampling rate and the quality of the analog signal to be converted, we only made use of one channel. A typical plot of acquired data is shown in Figure 3-36.

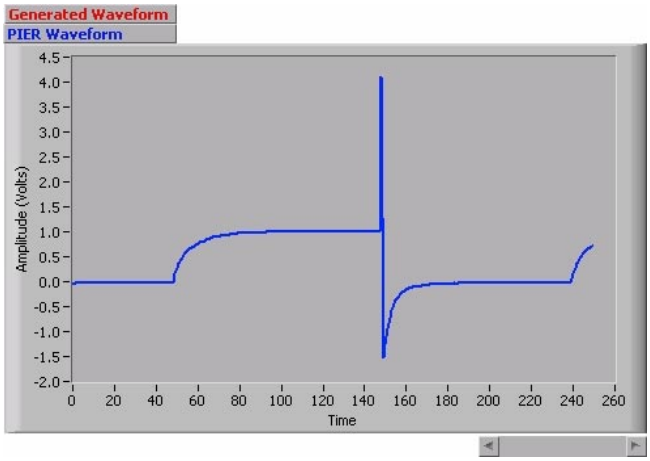


Figure 3-36
Typical data obtained by the LabVIEW emulator from the PIER sensor. The sharp peak at the end of the pulse is the discharge of the integrating capacitor.

In simulation the DAQ has no triggering option (the price for fast data acquisition). Thus, the data array is recorded randomly. We emulated the work of the processor that extracts data related to a single pulse.

This virtual instrument (VI) enabled us to control an output, process the input signals, and log the data. LabVIEW uses visual programming; i.e., it is programmed with a set of icons that represent controls and functions available in the menu of the software. The VI consists of two parts—a front panel and a block diagram. The front panel is fully customizable to include output controls, error messages, and knobs, and display graphs that would generally be seen on a typical measuring device such as an oscilloscope. Figure 3-37 is an example of the front panel view of our PIER monitoring system.

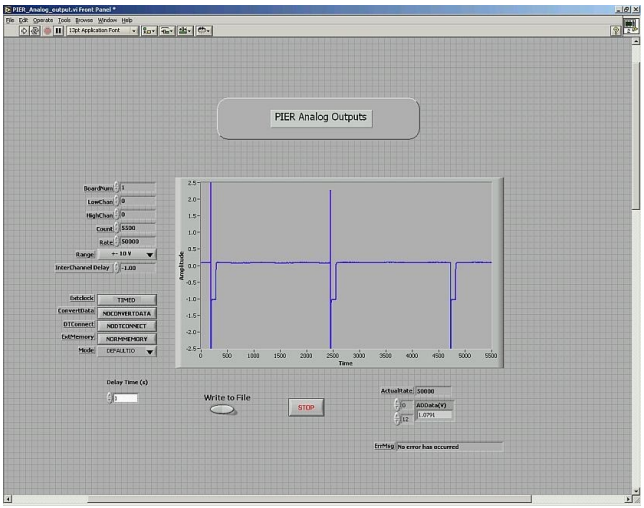


Figure 3-37
Front panel emulator of the virtual instrument that emulates the PIER processor.

The PIER front panel has several features and control buttons that allow us to specify the board number that we are using, the number of channels to be used, the sampling rate used in our conversion, the number of counts taken at our sampling rate, the voltage range of our personal DAQ, and the interchannel delay between various channels.

The particular VI that is associated with our emulator is AinScFg.vi (name of the file), which can be found in the universal library for measurement computing integrated into LabVIEW. This VI allows us to scan a range of A/D channels in the foreground and store the samples in an array. It also reads the specified number of A/D samples at the specified sampling rate from the particular board. In our case, we are using board number 1 at a sampling rate of 50,000 samples/second, with one A/D channel at a count of 3500 samples. A summary list of inputs and outputs associated with AinScFg.vi is provided below.

Inputs:

- BoardNum – the board number assigned to a particular DAQ. This number is assigned in the configuration of the DAQ through a software called InstaCal
- LowChan – First A/D channel of scan
- HighChan – Last A/D channel of scan
- Count – Number of A/D samples to collect
- Rate – Sample rate in scans per second
- Range – A/D range code
- Options – Bit fields that control various options
- InterChannel Delay – Delay in seconds between channels in a scan.

* Note: There are a total of eight channels that can be used in single-ended mode and four channels in differential mode. In our case, we are using single-ended mode.

Outputs:

- Rate – Actual rate the board is sampled
- ADData – Data array that stores A/D values
- ErrCode – Error code.

The parameters which we used for our monitor system are as follows:

- BoardNum is 1, specified through InstaCal. We use a LowChan of 0 only. We do not have a high channel because we are using only 1 channel
- The Count varies according to how much of the signal you would like to view. It ranges anywhere from 2500 to 5000 counts
- The Rate that we are sampling at is 50,000 samples/sec, and the A/D voltage range of our DAQ is set to ±10 V. This is the voltage range used in single-ended mode.

In our monitor system, we do not make use of the Options input, and the InterChannel Delay would not matter as well since we are only using one channel.

The front panel also contains a button to record real-time data obtained from one signal pulse of our waveform and store the information in a log file. This is a useful feature that will be used to obtain the dielectric permittivity spectrum by means of Fast Fourier Transform. Figure 3-38 is the PIER monitor system block diagram of the LabVIEW emulator.

As one can see from Figure 3-38, the block diagram is built mainly through graphical icons that are interconnected to provide the features observed on the front panel. All of the interconnected icons are situated in one ‘while’ loop. This is done to acquire and display data continuously until the stop button is activated. The main VI, AinScFg.vi, is situated on the left side of Figure 3-38. It is interconnected with other icons to display the controls and indicators for each input and output associated with this particular VI. The count specifies the total number of A/D samples that will be collected. If more than one channel is being sampled, the number of samples

collected per channel is equal to Count/(HighChan-LowChan+1). This is represented by the triangle icons on the upper left of the diagram. It is basically some small logic manipulation. All of the output data retrieved from the DAQ are in binary representations and need to be converted to engineering units, such as volts or amplitude. Therefore, we use a sub-VI called ToEng to convert this to appropriate units for interpretation. The Spectral Measurement VI will attain all the spectral parameters of the real and imaginary components of our waveform. This can be represented in either graphical or written form.

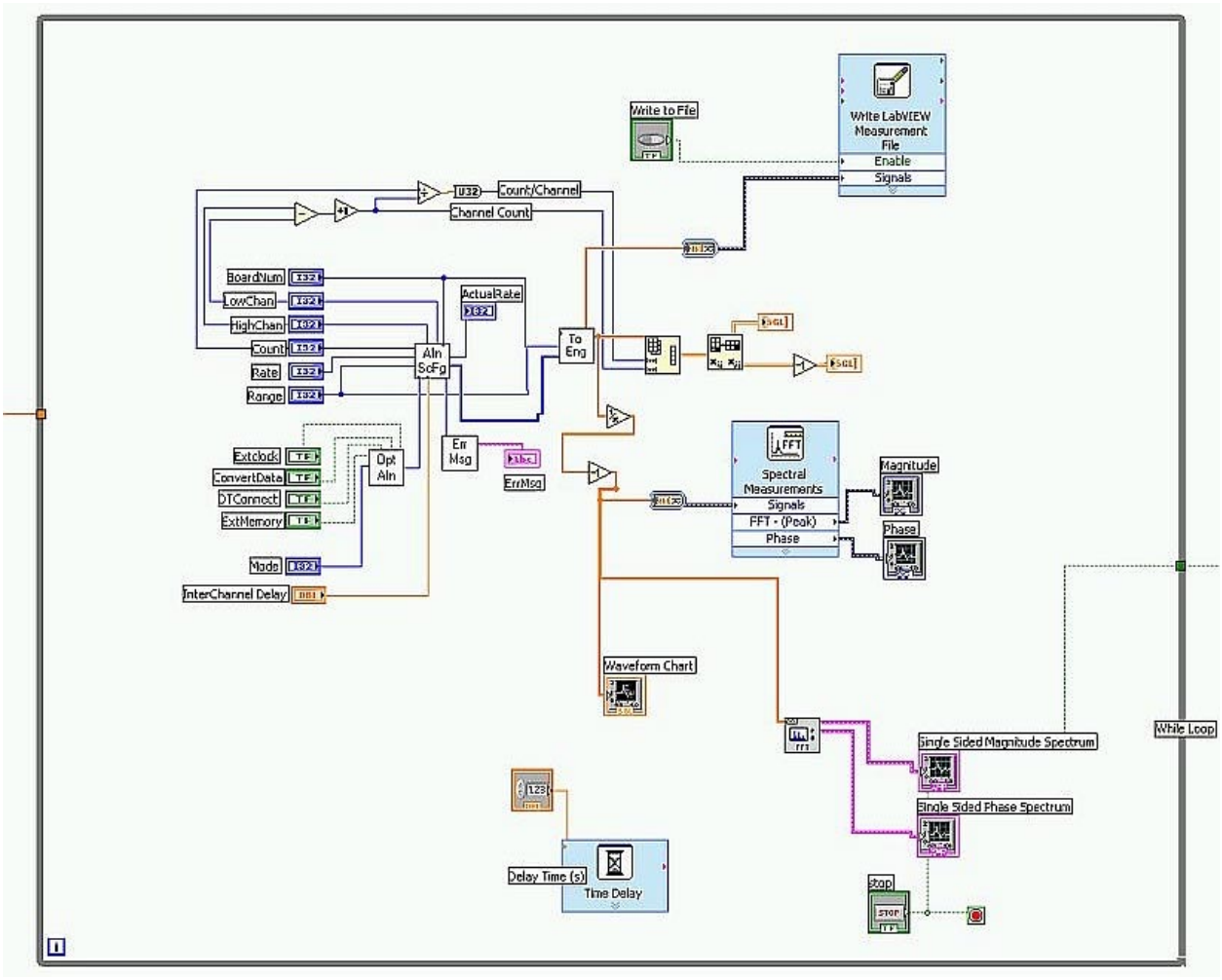


Figure 3-38
Virtual instrument that emulates the PIER processor.

All of the data that are converted into engineering units are later stored in an index array to be observed at the viewer's discretion. This array is also interconnected to another VI, called Write LabVIEW Measurement File.vi, to store all data retrieved from the DAQ in a log file. This VI is set so that data will be overwritten each time the button is activated. It can also be set to append data if the user so chooses.

3.2.9.2 Results of the Testing

The algorithm described in Section 3.2.8 was implemented in a MathCAD program, as shown in Listing 3-1. The program retrieves data from the text file, calculates the spectrum of dielectric losses and writes it as a text file.

Listing 3-1. MathCAD Program That Retrieves Data from the Text File, Calculates the Spectrum of Dielectric Losses, and Writes It as the Text File

PIER Algorithm Test by M.Reznikov

$k := 1 .. 2$ $\quad j := 0 .. 4499$ $\quad y := \text{READPRN}("H:\text{Contracts}\text{PIER II}\text{Tests}\text{test1}\text{five\_pct\_oil.txt}")$

$X_j := y_{j,1}$ $\quad s := 380$ $\quad u := 2000$ $\quad k := 0 .. 4095$ $\quad j := 1 .. 2048$

$b := \sqrt[2]{2}$ constant of logarithmic increment $\quad Xmax := X_u$ $\quad t0 := 2 \cdot 10^{-5}$ $\quad w_j := 2 \cdot \frac{\pi}{t0 \cdot j}$

$N := \log(4095, b) - \text{mod}(\log(4095, b), 1)$

$$XX_k := \begin{cases} (X_{k+s} - X_s) & \text{if } k \le u \\ Xmax - X_s & \text{otherwise} \end{cases}$$

$N =$ number of data

$i := 0 .. N$ time index $\quad t0 := 2 \cdot 10^{-5}$ minimal time

$n := 0 .. N$ frequency index $\quad t_i := t0 \cdot b^i$ time variable $\quad z_n := b^n - \text{mod}(b^n, 1)$

$m_i := b^i$

$q_0 := 0$

$$tf_i := \frac{\left[t_i - t0 \cdot \left[(m_i) - \text{mod}(m_i, 1)\right]\right]}{t0 \cdot \left[(m_i) - \text{mod}(m_i, 1) + 1\right] - t0 \cdot \left[(m_i) - \text{mod}(m_i, 1)\right]}$$

$$q_i := XX_{(m_i) - \text{mod}(m_i, 1)} + \left[XX_{(m_i) - \text{mod}(m_i, 1) + 1} - XX_{(m_i) - \text{mod}(m_i, 1)}\right] \cdot tf_i$$

$$w_n := \frac{(2 \cdot \pi)}{t0 \cdot b^n}$$ frequency variable

$$L_n := \frac{\sum_{i=0}^{N-1} (q_i - q_{i+1}) \frac{(\cos(w_n \cdot t_{i+1}) - \cos(w_n \cdot t_i))}{t_{i+1} - t_i}}{w_n}$$ output - losses

$Sp_{n,0} := w_n$ $\quad Sp_{n,1} := |L_n|$

$\text{WRITEPRN}("H:\text{Contracts}\text{PIER II}\text{Tests}\text{test1}\text{five\_pct\_oil\_sp.txt}") := Sp$

We tested four compositions of fluid:

(1) Pure mud
(2) Pure oil
(3) 50% oil in mud
(4) 5% oil in mud.

Also, the empty sensor chamber was tested to evaluate whether the polarization of sensor material significantly affects measurement. The spectra obtained are shown in Figure 3-39.

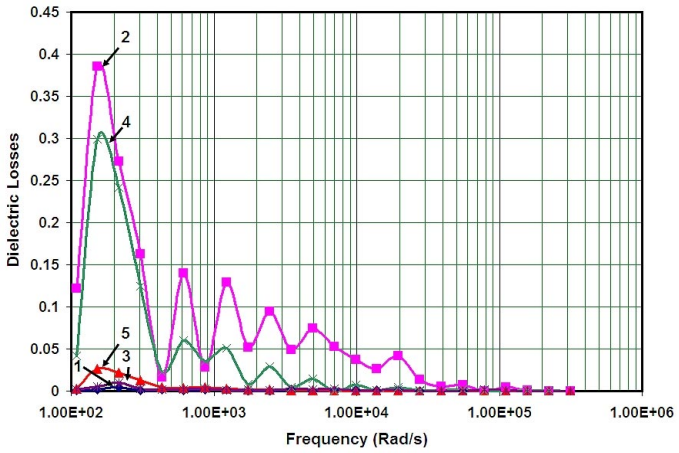


Figure 3-39
Calculated spectra of the effective dielectric losses measured with the PIER sensor. 1= empty chamber; 2 = pure oil; 3 = pure mud; 4 = 50% of oil in mud; 5 = 5% oil in mud. Nonmonotonous behavior of spectra results from the low sampling rate used in the DAQ.

Due to the limited sampling time used in the DAQ (20 μs), the spectra are not resolved at frequencies over 10^5 radians per second (rad/s). This allows us to suppress the fast polarization of electrolytes in the mud, thus highlighting the slow polarization of the oil that is of interest. Note that in the final prototype we used a sampling time over 100 ns to allow us to resolve frequencies up to 10^6 rad/s.

The oil peak around 150 rad/s corresponds to the relaxation time of 7 ms. This peak exists in all spectra of oil-containing fluids (curves 2, 4, and 5 in Figure 3-39). The low-frequency peak in the spectrum of pure mud (curve 3 in Figure 3-39) is located near 200 rad/s and has relatively low magnitude. The spectrum of the empty sensor (curve 1 in Figure 3-39) is negligible.

The dependence of the peak of oil-related losses (at 150 rad/s) to the oil content is plotted in Figure 3-40.

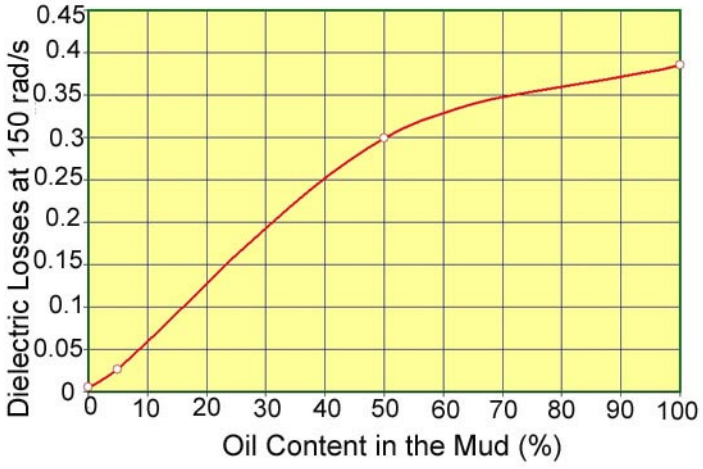


Figure 3-40
Dielectric losses in peak at 150 rad/s at varied content of oil in the mud.

As one can see from Figure 3-40, the target detection of 1% oil in mud has been achieved in this intermediate test. Therefore, the analog electronics of the PIER sensor meet the requirements.

3.3 PIER II (Final Prototype) Design

The final PIER prototype (PIER II) was built on the basis of a significant redesign of the preliminary prototype, PIER I. In this final prototype we have improved the rise time of the voltage pulse (from 300 ns to 9 ns), eliminated the delay between the start of data acquisition and the voltage pulse, implemented the logarithmic scale of data acquisition and the measurement of initial voltage offset on the integrator. Electronics and sensor (electrodes) are assembled into a rugged, slim construction installed on a single aluminum rail. Thus the PIER design accommodates the downhole application.

3.3.1 General Description

The PIER system is electrical hardware that consists of three functionally independent modules: an adjustable power supply, a data acquisition and processing system, and a signal integrator. Each of these modules performs a well-defined function that is independent of the remaining modules. The block diagram (Figure 3-41) illustrates the electrical connections between the modules. Also shown are external components (a power source, personal computer, and sensor) that complete the system.

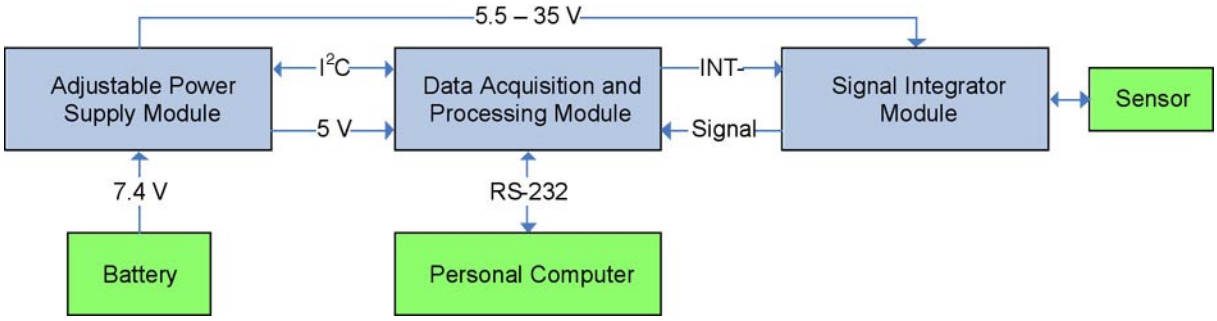


Figure 3-41
PIER II block diagram.

A general overview of how the PIER system operates is given below. Technical details have been purposely omitted to provide an easy-to-understand summary of overall operation.

Once the system is powered on and has initialized itself, it operates as follows:

1. The data acquisition module produces a periodic timing signal INT-. This timing signal partly controls data acquisition, but is primarily used by the signal integrator module to control integration of the sensor signal.
2. Depending on the state of INT-, the signal integrator integrates its sensor input and provides it as output, labeled 'Signal' in Figure 3-41, to the data acquisition module.
3. The data acquisition module performs high-speed sampling and analog-to-digital conversion of the analog input signal. The voltage range of the analog signal is monitored and commands are later sent (via the I2C interface) to the power supply module to adjust the voltage to the signal integrator.
4. Once the analog signal for an INT- period is completely received, it is processed in digital form. Information obtained from the processing is output to a personal computer via a standard serial RS232 interface. Commands to adjust the voltage to the signal integrator are sent to the power supply module.
5. Operation repeats from step 1.

The data acquisition and processing module is the core element of the PIER system. It is responsible for:

- Providing an interface to a personal computer for receiving commands and outputting data to a user.
- Monitoring the received analog signal voltage range and appropriately commanding the adjustable power supply so that the full range of the ADC is utilized, without saturation.
- Generating and responding to precise timing signals to control data acquisition.
- Complex signal processing of the received data, including a Fourier transform of unevenly sampled data, and analysis of the resulting frequency spectrum.

The main hardware components of the data acquisition and processing module are:

- A Microchip dsPIC30F6015 microcontroller that generates the timing signals used by other components and modules, provides an interface to a personal computer, stores and processes sensor data, and commands the adjustable power supply.
- An Analog Devices AD9220 that performs 12-bit A/D conversion of the analog input signal at 10 MHz. The output of the AD9220 is fed into an IDT72275 64k FIFO, from which the microcontroller receives its data.
- An Altera PLD that responds to timing signals and commands generated by the microcontroller. The PLD generates the INT- signal for the signal integrator module, and controls read and write operations to the FIFO, allowing correctly timed sensor samples to be read by the microcontroller.

3.3.2 PIER Microcontroller Software Overview

A flowchart of the microcontroller software is shown in Figure 3-42. The microcontroller begins program execution at “Start”. After hardware and software configuration is complete, the program enters an infinite loop consisting of a state machine (orange rectangle) with four states (blue rectangles), followed by one additional function call.

At each cycle through the main loop, only the current active state is executed within the state machine. Transitions among the four states are indicated with directed arrows. If the state transition depends on the occurrence of an external event, it is labeled as such.

The function “CalculateOilContent()” is responsible for frequency domain analysis of the data received. The majority of mathematical operations involved operate on vectors and matrices of 16-bit fractional data (floating point numbers in the range -1.0 to + 1.0).

The Fourier transform has been implemented as a matrix operation, and while this is not computationally efficient, it was necessary as the data collected had been unevenly sampled in time. The use of 16-bit fractional numbers enabled the use of fast (Assembly language) routines for numerical computation, and was also the most logical choice of data type as the microcontroller data bus is 16 bits wide. A summary of the signal processing algorithm and its output was presented in Section 3.1.3.

3.3.3 PIER Computer Interface, Initialization, and Operation

The PIER system receives commands and provides data output via a standard RS232 serial communications link to a personal computer. This communications interface is provided by the data acquisition and processing module.

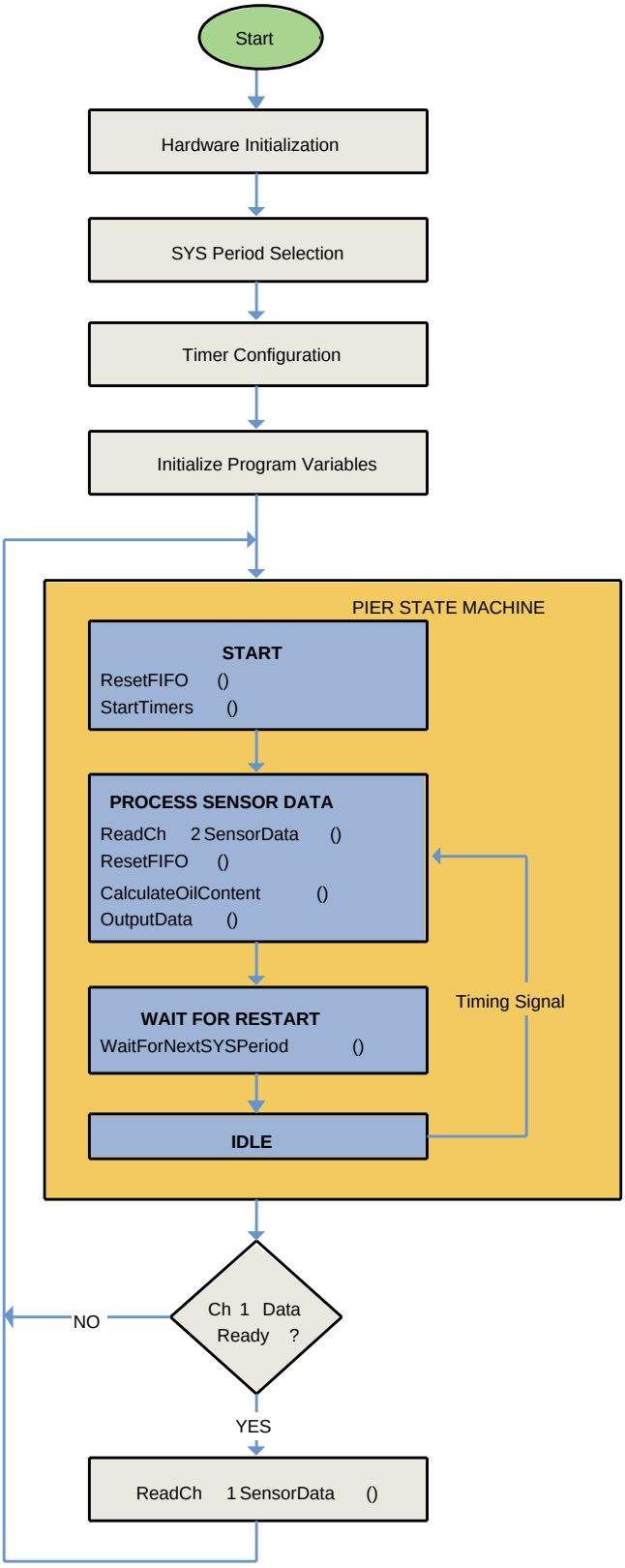


Figure 3-42
A flowchart of the PIER II microcontroller software.

In general, any serial port communications or "terminal" program that allows standard ASCII data to be sent and received could be used. In the development of PIER, Windows HyperTerminal was used. The necessary communication settings are:

- Baud rate: 57600 bps
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None.

Once the data acquisition and processing module is connected to a computer and powered on, the terminal program should display:

PIER: Hardware initialization complete...
Please select desired SYS period...
1 = 20 ms
2 = 200 ms
3 = 2000 ms
SYS period:_

At this point the user is required to select a period for the primary timing signal known as SYS. The user selects the desired SYS period by entering 1, 2, or 3. Once a period has been selected, there is a brief pause as the system calculates parameters needed for data processing. The terminal program should eventually display:

PIER: Data processing initialization complete...
PIER: SYS timing configuration complete...
PIER: Program variables initialized...
PIER: Running...

At this point the PIER will begin normal operation. The system will output at periodic intervals a single number resulting from analysis of the received data. In the following output the values are fabricated, but correctly indicate the format of the output.

percentageOil = 57.38
percentageOil = 56.93
etc.

3.3.4 Data Acquisition Board

This section describes the operation and software requirements for the Microchip dsPIC30F6015 digital signal controller, or dsPIC, which interfaces to the data acquisition hardware of the PIER II data acquisition board assembly. The dsPIC communicates with a controlling computer via an RS232A serial interface and with an adjustable power supply via its interintegrated circuit (I^2C) module.

3.3.4.1 Operation of Data Acquisition Board

The system block diagram in Figure 3-43 shows the major components of the data acquisition system.

The data acquisition system is operated synchronously, with all clocked devices receiving the same clock signal, 10MCLK. That clock signal is generated by the dsPIC, which divides its incoming clock by 4 and outputs the lower frequency clock at its CLKOUT pin. The dsPIC also uses the lower frequency clock for its internal clock cycle. 10MCLK is a 10 MHz clock, and therefore the dsPIC executes at a 10 MIPS (mega instructions per second) rate.

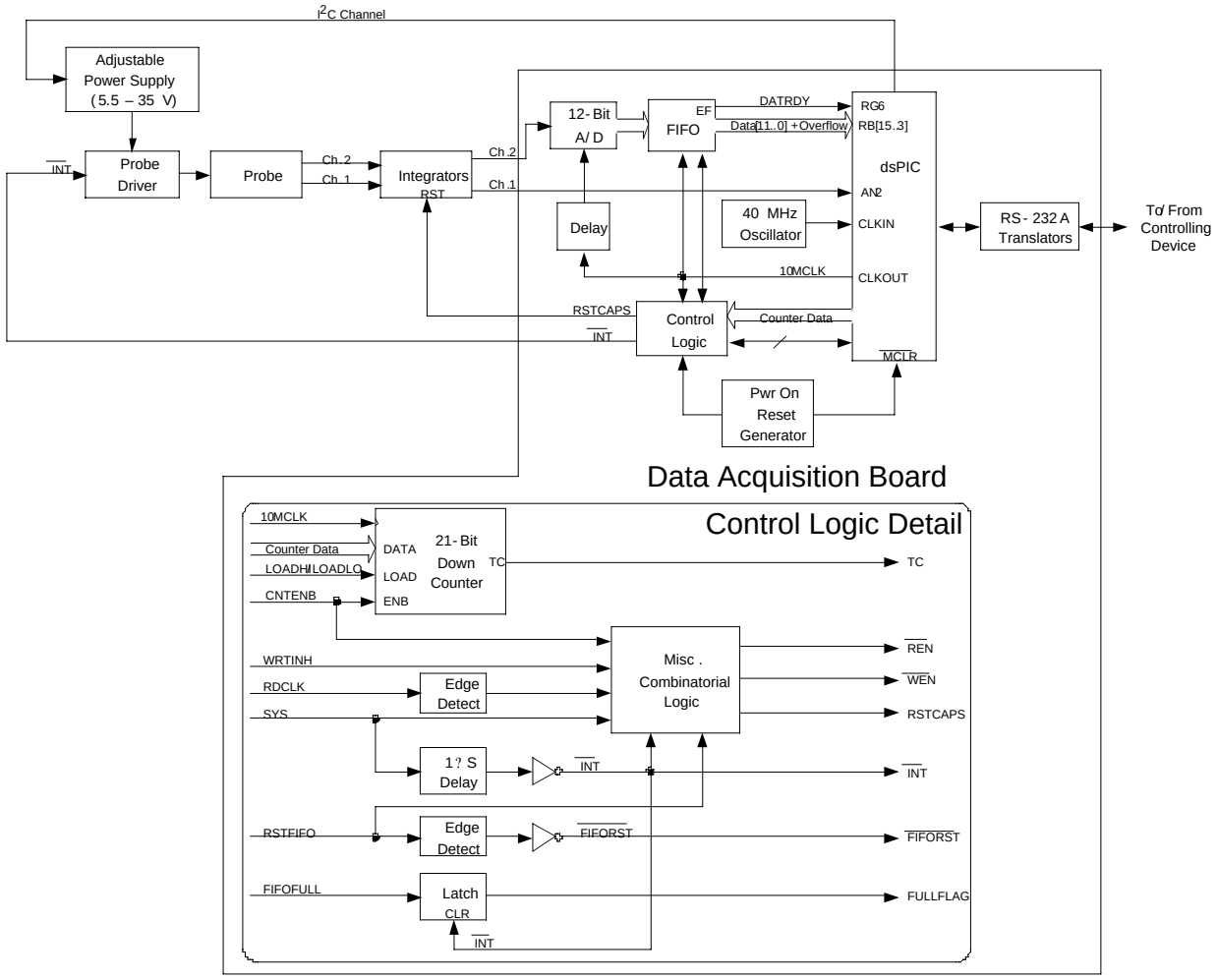


Figure 3-43
PIER II hardware block diagram.

As an overview, the system operates as follows: a dual-channel capacitive probe is charged by the probe driver to the voltage set by the adjustable power supply. The voltage rise in the probe is integrated, one integrator for each channel. The output of each integrator is digitized by analog-to-digital converters, and selected data from each channel are collected and stored by the dsPIC. Although the two integrators are identical, the required resolution for their digitizers is not. Channel 2 requires digital data with 12-bit precision, and samples must be taken precisely at 100 ns intervals. Channel 1 requires much less precision (eight bits is sufficient) and samples may be taken at nonspecific intervals, though the approximate place in the system cycle is important.

The integrator output is a rising exponential waveform that begins when a timing signal called INT- goes low. Being an exponential, it rises toward an asymptote called “saturation.” Nearing that point, the waveform has an imperceptible slope, and is essentially horizontal. Another region of interest is the “baseline,” which is the portion of the waveform just before it begins to rise (see Figure 3-44). Both the baseline and saturation regions will be referred to in several of the sections that follow.

The Channel 2 A/D runs constantly, outputting its data to a FIFO buffer, that is controlled by system timing to accept data only at a specific time in the cycle. Moreover, only certain data

samples must to be kept by the dsPIC. Since the dsPIC is not fast enough to do the sorting operation at the 100 nS data rate, custom control logic "throws away" the unneeded data by clocking the output side of the FIFO at high speed until a valid data sample appears at the FIFO output. At that time, the control logic informs the dsPIC to collect and store the data sample.

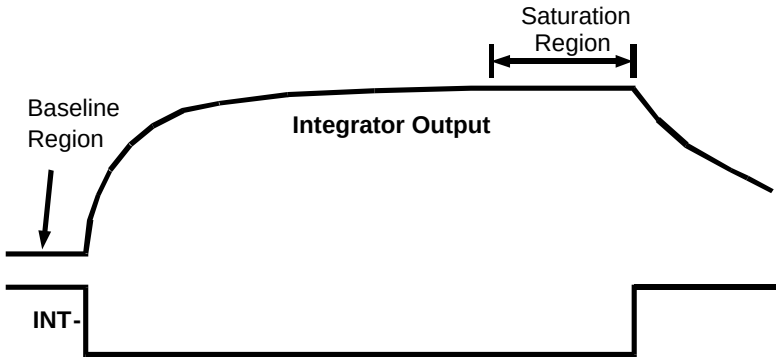


Figure 3-44
Integrator output signal.

The Channel 1 A/D is contained within the dsPIC, which monitors the system timing waveforms and digitizes data points only during baseline and saturation times. This is a much simpler and slower operation than that required for the other channel, so no external high-speed hardware is required.

3.3.4.2 System Timing

System timing is based on a signal called **SYS**, a free-running 25% duty cycle digital waveform with one of three possible periods: 20, 200, or 2,000 ms. The one that is in use is called the active period. SYS is generated by one of the PWMs in the dsPIC. We shall call SYS the primary timing signal. A secondary timing signal, **INT-**, is generated by the control logic. It is simply an inverted version of SYS, delayed by 1 μs.

The timing diagram (Figure 3-45) shows the two system timing waveforms and identifies the locations in the cycle of major events that must occur during the cycle. Except for the relationship between duty cycle and period, the drawing is not to scale. In particular, the 1 μs delay between SYS and INT- is exaggerated for clarity.

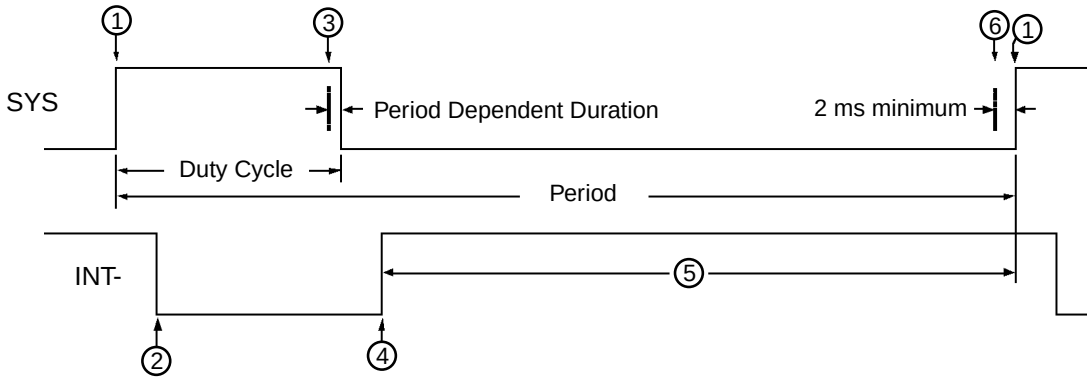


Figure 3-45
PIER II data acquisition event timing.

3.3.4.3 Overview of Event Descriptions

The various major events are identified by the circled numbers in the timing diagram above.

Event 1 - SYS Goes High – Begin Writing Channel 2 Data to the FIFO. When SYS goes high, the control logic enables Channel 2 digitized data to be written to the FIFO. The first 14 words are the "baseline" data. They represent the idle state of Channel 2 and are collected, then averaged, and the average is stored for later use. Also at this point, the dsPIC must start a timer to identify the event ③ location (in time). The timer duration will depend on the length of the active period.

Event 2 - INT- Goes Low – Begin Data Collection. After the last baseline data word is collected, the remainder of the samples in the FIFO are integrator data samples. Only a tiny fraction of the tens of thousands of such samples will be collected and stored by the dsPIC, and the process for doing that were discussed in detail in Section 3.3.4.4 and its subsections. Note that the dsPIC need not identify the falling edge of **INT-**. It merely counts the baseline words collected, and the 15th word is the first integrator data sample. It just happens to coincide with the falling edge of **INT-**.

Event 3 - Timer started at Event 1 Expires – Collect Channel 1 Saturation Data. The dsPIC onboard A/D module digitizes about eight to ten Channel 1 saturation samples in the last couple of milliseconds of the SYS high time. These are averaged and stored for later use. Note that Channel 2 saturation samples are identified and collected by other means, described in Section 3.2.4.2.

Event 4 - INT- Goes High – No More Saturation Data, Reset Capacitors, Set Timer. Occurring 1 μs after the falling edge of SYS, this point marks the time before which the last saturation word must be sampled. The control logic automatically resets the integration capacitors by asserting the **RSTCAPS** signal, causing the waveform to begin to fall (as suggested in Figure 3-43). This is also a good time to start a timer, which upon expiring will mark the event ⑥ point. Also at this time, the control logic automatically disables writing of Channel 2 data to the FIFO.

Event 5 - The Reset Interval. During this interval the **RSTCAPS** signal continues to be applied to the integrators, causing the capacitors to drain their charge. It takes well over 100 μs for this to happen.

Event 6 - Timer Started at Event 4 Expires – Collect Channel 1 Baseline Data. The dsPIC onboard A/D module digitizes about eight to ten Channel 1 baseline samples in the last couple of milliseconds of SYS being low. These are averaged and stored for later use.

3.3.4.4 System Tasks

Numerous system tasks are assigned either to the control logic or to the dsPIC. Some control logic tasks operate independently of the dsPIC, while others are a response to a signal, or command, from the dsPIC. Still other tasks are performed by the dsPIC without involving the control logic at all. All types of tasks, except for the generation of SYS itself, are triggered from the main timing signal, SYS, INT-, or as a result of a timer (initiated at a SYS edge) expiring.

The high-speed control logic accepts "commands" from the dsPIC and cues from the system timing signals, then does the following:

- Controls when data is written into and read out of the FIFO
- Counts the Channel 2 data samples that are to be skipped and discarded and notifies the dsPIC when to collect a valid sample
- From the primary system timing signal, SYS, creates the delayed, secondary system timing signal, INT-
- Generates the required signals to reset the FIFO upon dsPIC command

- Resets the integrator capacitors at the correct time in the cycle
- Monitors the "FIFO Full" flag and latches it if it should ever occur during a cycle
- Inhibits writing to the FIFO upon dsPIC command.

Many of these tasks are results from a command from the dsPIC.

3.4 PIER Communication Procedures

3.4.1 Communication with Host

A controlling device, or host (computer), communicates with the dsPIC via an RS232A interface. The communication module in the dsPIC contains two UARTs, and the hardware is configured to utilize UART1 for this function.

3.4.2 Communication with Power Supply

The adjustable power supply is controlled with the dsPIC via its built-in two-wire I^2C interface. The pins for this module are shared with RG2 and RG3; however, in this application those pins are dedicated to the I^2C function.

Only two devices reside on this I^2C bus: the dsPIC as the master, and an AD5259 digital potentiometer as the slave (seven-bit address 0011000). The I^2C standard allows one of two SCL (clock) frequencies: 100 kHz or 400 kHz. The lower frequency is recommended for this application, since speed is not a critical need here and the fewer high-frequency signals in the system, the better.

The power supply output voltage is controlled by writing an eight-bit value to the slave device. The output voltage is determined by equation VOUT = 34.85 – 0.2299 × Data, where "Data" is the eight-bit value. Of the several commands supported by the AD5259, only two will be used in this application. Writing to the EEPROM register will be executed in the initialization routine of the dsPIC. A data byte of 128 will be loaded to that register at power up, setting the power-supply output to the default 5.5 volts. Any writing after the first one (occurring on subsequent power-up cycles) are redundant, but harmless.

The other command is "Writing to the RDAC register". This command is executed when the dsPIC must change the power supply output voltage. The desired power supply output voltage is substituted for VOUT in Eq. (3-24), and the equation is solved for "Data". The data is rounded to the nearest integer and sent to the AD5259. The I2C data format for each command is shown in Figure 3-46.

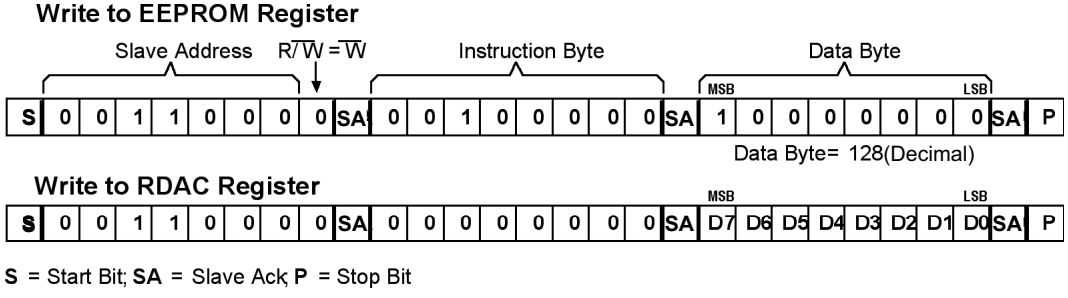


Figure 3-46
Digital port command formats.

Sending a command to the power supply requires that three bytes be loaded sequentially into the I2CTRN register of the I^2C module in the dsPIC. The first byte is the slave address, and it is always the same. The second byte is the instruction byte, which is all zeroes except for bit 5 in the EEPROM command. The third byte is the data variable for the RDAC instruction, and fixed at 128 (80 H) for the EEPROM instruction.

3.5 Generate and Monitor SYS

Three versions of SYS are required in this application. All versions consist of a 25% single-pulse duty cycle, but the versions differ by period (see Figure 3-44). The periods required are 20, 200, and 2,000 ms. The durations of the corresponding 25% duty cycle pulses are 5, 50, and 500 ms, respectively. The dsPIC is commanded as to which version to use via the host interface (the RS232A interface).

The SYS signal exits the dsPIC on the RE1/PWM1H [output] pin, so it would be convenient to create SYS with the PWM module. Using that resource, the period and duty cycle can be set once, and it will free run without requiring further software attention, including interrupts. However, SYS must be monitored to detect the key events that must be generated by the dsPIC. Therefore, SYS is also connected to [input] port pin RG7/CN9, which can be programmed to generate an interrupt upon any change of state of SYS. As mentioned earlier in Section 3.3.4.2, each time SYS changes state, a timer must be set to mark the time to collect baseline or saturation samples.

3.6 Digitize and Store Channel 1 Data

The dsPIC onboard A/D converter is used to digitize data from the Channel 1 integrator. The analog signal enters the chip at port pin RB2/AN2. The A/D module should be configured to digitize samples as quickly as possible, as only a few hundred microseconds (for the saturation samples of the 20 ms period) are available in which to perform the operations.

As illustrated in Figure 3-45, these conversions are performed at the end of the SYS high time (saturation samples) and at the end of the SYS low time (baseline samples). About eight to ten samples of each are sufficient to calculate a reliable average. Unlike Channel 2, no other samples must be collected from Channel 1.

3.7 Collect and Store Selected Digitized Samples from Channel 2

This is by far the most complicated task in this application. It involves precise bidirectional communication between the dsPIC and the control logic. Ignoring all the tasks that have nothing to do with Channel 2 data collection, the sequential steps in this procedure are:

- The control logic enables continuous data from the Channel 2 A/D converter to be written to the FIFO when SYS goes high. There is one conversion and one write to the FIFO every 100 ns.
- Shortly after the first data word is written to the FIFO, it appears at the FIFO output. The dsPIC is signaled that the FIFO is ready to read.
- The dsPIC performs a clock-read operation for the first nineteen contiguous data words. A clock-read operation consists of pulsing the read clock (RDCLK on the schematic), then reading a data word that is at the dsPIC's FIFO data port (RB[14..3]). The first fourteen words are baseline data, the next five are integrator data words 1 through 5.
- The next two words need not be collected, so the dsPIC pulses the read clock twice, but does not read the data, thereby discarding those two words (6 and 7).
- The dsPIC performs a clock-read operation for integrator data word 8, then discards the next two (words 9 and 10) by performing two read clock (only) operations.
- The dsPIC performs a clock-read operation for integrator data word 11, and now things change. The next integrator data word to be collected is 16, so there are four words to skip (12-15). The dsPIC loads a "5" to the "Skip Counter" in the control logic (the 21-Bit down counter in Figure 3-43), instructing it to pulse the FIFO read clock four times at high speed.

- When the control logic has finished discarding words 12 through 15, it signals the dsPIC that a new word is ready to read. The dsPIC then performs a read operation (without the clock preceding it) for integrator data word 16.

This "skip many, read one" sequence of operations continues until the last valid integrator data word is read. With each word read, the number of words to be skipped and discarded increases. The skip number becomes quite large by the end of the SYS high time; it is 21 bits at the end of the longest SYS duty cycle.

After the last sample has been collected, a period-dependent number is loaded to the skip counter, discarding all remaining integrator samples except for the last few. These are the Channel 2 saturation samples. Eight to ten of these are collected samples, and their average is taken and stored for later use; refer to Tables 3-4 and 3-5 for details.

Table 3-4. List of the Channel 2 Integrator Data Words to be Collected

For 20 ms Period			
Sample Number	Data Number	Sample Number	Data Number
BL1-14	N/A	16	256
1	1	17	362
2	2	18	512
3	3	19	724
4	4	20	1,024
5	5	21	1,448
6	8	22	2,048
7	11	23	2,896
8	16	24	4,096
9	22	25	5,792
10	32	26	8,192
11	45	27	11,585
12	64	28	16,384
13	90	29	23,170
14	128	30	32,768
15	181	31	46,340

For 200 ms Period add …			
Sample Number	Data Number	Sample Number	Data Number
32	65,536	35	185,363
33	92,681	36	262,144
34	131,072	37	370,727
For 2,000 ms Period add …			
Sample Number	Data Number	Sample Number	Data Number
38	524,288	42	2,097,152
39	741,455	43	2,965,820
40	1,048,576	44	4,194,304
41	1,482,910		

Note: There are three sections, one for each possible SYS period. For a 20 ms period, 14 baseline data words are collected (BL1-14), followed by 31 Integrator samples.

Table 3-5. Sampling in PIER II

Period	Last Sample Number	Skip Count
20 ms	31	3,600
200 ms	37	128,000
2,000 ms	44	780,000

The skip counter in the control logic can be programmed to skip any number of data words from 1 to 33,554,431. However, at very low numbers, it would take more time to load and start the process than to command single read-clock pulses of the FIFO. The author arbitrarily selected 4 as the threshold for switching the skipping method from single read-clock pulses to the

automatic high-speed logic. The programmer may select his/her own threshold if desired. Alternately, he/she may decide to put the whole thing in a single loop, using the automatic logic to skip even a single data word.

Table 3-4 shows the means for calculating the skip count. The sample number is the number of integrator data samples actually collected (after the last baseline sample), whereas the data number is the number of the sample converted and written to the FIFO (again, after the last baseline sample). Most of the data number samples are discarded. For example, if Sample 7 has just been collected, its data number is 11. The number to be loaded to the skip counter is obtained by subtracting the current data number from the next data number, e.g., 16–11 = 5; therefore this skip number is 5. As another example, Sample 37 has just been collected, but the active period is 2,000 ms, so there are more samples to collect. The calculation becomes 524,288–370,727 = 153,561, which is loaded to the skip counter. Remember, when using the skip counter to get to the next data number to be collected; the reading of the FIFO data is not preceded by a read-clock operation. The skip counter automatically performs all the clocking that is necessary.

When a 200 ms SYS period is used, six more samples are collected. And for the 2,000 ms period, seven more samples are collected, for a total of 44 plus the 14 baseline samples. Note that as mentioned before, the difference between samples 43 and 44 is quite large (a 21-bit number; 12BEC4H).

The saturation samples are converted at the end of the duty cycle, and therefore are the last samples in the FIFO. After the last integrator sample has been collected and stored, the skip counter must again be used to move quickly to the samples converted during that time. Table 3-5 gives the number to be loaded to the skip counter for each period. Note that it is certain that the saturation samples will actually be collected well after the duty cycle has expired. Therefore, other dsPIC tasks must be allowed to continue in parallel with this activity. Specifically, but not exclusively, the falling edge of SYS must not be allowed to occur unnoticed, as there are actions that must occur at that time.

3.7.1 Hardware Resources for Data Collection

There are several hardware resources available to the dsPIC to allow for the easy collection of the required selected Channel 2 data words. This section describes the details of the data collection scenario presented in Section 3.7, including what the resources are, how they work, and which pins on the dsPIC are used for each.

3.7.1.1 FIFO Data Interface

The FIFO buffers the 12-bit data from the Channel 2 A/D converter to the dsPIC. The FIFO data FDAT[11..0] enters the dsPIC at [input] pins RB[14..3], respectively. There is an overflow bit associated with each data word. For convenience, it has been located on the same port as the FIFO data bus, at RB15. If the A/D converter reports that a sample is out of range, the overflow bit associated with that sample will be high. Should the overflow bit ever be found to be high, it invalidates the entire cycle of data collection. The data is discarded, the power supply voltage is reduced, and a new data collection sequence starts at the beginning of the next cycle.

3.7.1.2 FIFO Control Interface

When a new cycle starts, the FIFO will be empty. Writing to the FIFO commences automatically as described in Section 3.3.4.3. It takes a short time for the data to fall through to the output of the FIFO. When data is available at the read (output) port, a data ready flag (DATRDY) goes high at dsPIC [input] pin RG6. At that time, the dsPIC may begin read operations as outlined in Section 3.7.

The FIFO is very deep (65k words) and should never become full if the software to empty it is efficiently written. The key is to collect a data word and load the skip number into the control logic as quickly as possible. Data is being written to the FIFO every 100 ns. When the skip counter is active, data is being read and discarded at the same rate, so the FIFO gets no fuller during that time. But when the dsPIC has control of the FIFO, it fills very fast. Therefore, code efficiency is important. If the FIFO ever were to become full, data could not be written to it and the validity of any further data reads cannot be guaranteed since some of the data remaining in the FIFO will be in the wrong place. A latched flag, FULLFLG, is available on dsPIC [input] pin RF6. If the FIFO becomes full at any point during the time when data is being written to it, the FULLFLG is latched in the high state and remains until INT- goes low again.

The control logic automatically enables writing to the FIFO from the time SYS goes high until the time when INT- goes high. If at any time during that interval it becomes necessary to stop writing to the FIFO, the dsPIC has been provided with a write inhibit control, WRTINH, at [output] pin RE5. It should be initialized to the low state and set high to inhibit automatic writes to the FIFO.

Before starting a new data collection cycle it will be necessary to reset the FIFO, i.e., empty it. RE6 is the RSTFIFO pin, and it is a normally low output pin. Resetting the FIFO requires that this pin be high for a minimum of one instruction cycle, but longer is acceptable, as the control logic conditions the signal and responds only to the leading edge of the pulse. Ideally, the pin can be set, then cleared, with consecutive instructions, but if interrupted while the pulse is high (resulting in a longer pulse), no harm will ensue. This function is used to empty the FIFO during the low time of SYS, when it is known that the next SYS high time will begin a data collection cycle. The FIFO must be empty when new data begins being written to it again.

The data reading scenario outlined in this section described an operation wherein the read clock is pulsed. This is done by setting the normally low RDCLK [output] pin (RE7) high, then returning it to the low state. This pin must be high for a minimum of one instruction cycle, but longer is acceptable, as the control logic conditions the signal and responds only to the leading edge of the pulse. Ideally, the pin can be set, then cleared, with consecutive instructions, but if interrupted while the pulse is high (resulting in a longer pulse), no harm will ensue.

3.7.1.3 Skip Counter Interface

The skip counter is the 21-bit down-counter found in the control logic detail of Figure 3-42. When it is loaded with a nonzero number and counting is enabled, it counts down (toward zero) at a 10 MHz rate. For each count, the FIFO read-clock is pulsed once. When the counter reaches zero, counting automatically stops and its normally low terminal count signal, TC, goes high. The dsPIC reads TC at its input pin RD11, which conveniently, but not accidentally, is an external interrupt pin, INT4. The counter remains halted at zero with TC high until a new, nonzero number is loaded to it.

The skip counter is loaded via an 11-bit data path CNTRDAT[10..0] on dsPIC [output] pins RD[10..0], respectively. Obviously, an 11-bit data path is insufficient to carry 21 bits of data, so for data larger than 11 bits, the counter load is accomplished by first loading the lower 11 bits, then loading the upper 10 bits. The LOADLO command resides on dsPIC [output] pin RE3, and the LOADHI command resides on dsPIC [output] pin RE4. Both of these pins are active high and both must remain high for a minimum of one instruction cycle.

The dsPIC also controls the skip counter's ability to count via a count enable signal, CNTENB, located on [output] pin RE2. When CNTENB is low, counting is inhibited. When high, counting is enabled. A skip counter load operation proceeds as follows:

1. CNTENB is brought low to prevent the skip counter from "taking off" when the low data is loaded.
2. The low data are sent to the output port, CNTRDAT[10..0].
3. LOADLO is pulsed high, then low. Loading the lower 11 bits also clears the upper 10 bits of the counter. This is a handy feature, eliminating the need for a high load sequence for data of 11 bits or less.
4. For counter data larger than 11 bits, the high data is placed on the output port, CNTRDAT[9..0], then LOADHI is pulsed high then low. As pointed out above, this step is optional if the high data is zero.
5. CNTENB is set high and other actions are carried out until TC is high.

3.7.2 dsPIC Configuration Settings

Table 3-6 lists all dsPIC pin assignments that have an impact on software design. The initial state of all output pins not assigned to an internal controlling module is "0". The Comm and PWM modules control their own pins as soon as they are initialized. Virtually all of the pins on the dsPIC serve multiple functions, and the active function is program dependent. The entries in the dsPIC pin column note the register-bit ID and the function used, if any.

Table 3-6. List of dsPIC Pin Assignments

Name on the Schematic	dsPIC Pin	In, Out or BiDir	Main Ref. Section	Description
40MCLK	OSC1/CLKIN	IN	4.3	40 MHz external clock input with no PLL = 100 ns instruction cycle
CNTENB	RE2	OUT	3.2.4.3.3	Enables the skip counter to count
CNTRDAT[10..0]	RD[10..0]	OUT	3.2.4.3.1	11-bit data bus to load the 21-bit skip counter (in two operations)
DATRDY	RG6	IN	3.2.4.3.2	Goes high when data is available at the output of the FIFO
FDAT[11..0]	RB[14..3]	IN	3.2.4.3.2	12-bit FIFO output data bus
FULLFLG	RF6/INT0	IN	3.2.4.3.2	Latched FIFO full flag
INT1	RB2/AN2	IN	3.2.3, 4.4	Analog input from Channel 1 Integrator
LOADLO	RE3	OUT	3.2.4.3.3	Loads CNTRDAT[ ] into the skip counter's low bits
LOADHI	RE4	OUT	3.2.4.3.3	Loads CNTRDAT[ ] into the skip counter's high bits
RCV	RF2/U1RX	BiDIR	3.2.1.1, 4.6.2	RS232A receive channel
RDCLK	RE7	OUT	3.2.4, 3.2.4.3.2	Clocks the FIFO read port once for each RDCLK pulse
RSTFIFO	RE6	OUT	3.2.4.3.2	Empties the FIFO of all data
SCL	RG2/SCL	OUT	3.2.1.2, 4.6.1	I^2C clock, used for communication with adjustable power supply
SDA	RG3/SDA	BiDIR	3.2.1.2, 4.6.1	I^2C data, used for communication with adjustable power supply
SYS	RE1/PWM1H	OUT	Everywhere	Main system timing signal
TC	RD11/INT4	IN	3.2.4.3.3	Skip counter terminal count
WRTINH	RE5	OUT	3.2.4.3.2	FIFO write inhibit, overrides automatic writing
XMIT	RF3/U1TX	BiDIR	3.2.1.1, 4.6.2	RS-232A transmit channel

Timers must be set at Event 1 (called Timer 1) and at the falling edge of SYS (Timer 2). Since they do not run simultaneously, they can be the same physical timer or different ones, at the programmer's option. The purpose of Timer 1 is to mark the saturation sample collection time for Channel 1 (Channel 2 saturation samples are identified by other means), and Timer 2 marks the time for collecting baseline samples for Channel 1 (Channel 2 baseline samples are written to the FIFO automatically).

The times should be set as follows:

- For a 20 ms period, set Timer 1 to 4.85 ms and Timer 2 to 14 ms.
- For a 200 ms period, set Timer 1 to 49 ms and Timer 2 to 149 ms.
- For a 2,000 ms period, set Timer 1 to 499 ms and Timer 2 to 1499 ms.
- For all timer settings except Timer 1 for the 20 ms period, 1.1 ms is available to convert, average, and store eight to ten samples. That is more than enough time. For Timer 1 at the 20 ms period, only 151 ms is available. This is still more than enough time to convert and store the samples, but requires that the A/D module be configured for very fast conversions.

The dsPIC is clocked by an external 40 MHz clock oscillator and is divided by 4 to create the internal 10 MHz clock (TCY = 100 ns). The 10 MHz clock is also output from the chip on the OSC2/CLKOUT pin for use by the rest of the system. The only oscillator mode that supports this operation is EC, and that is the one to use.

The A/D module receives its only input at AN2. VREF- is grounded and VREF+ = 4.50 V, supporting the expected range of analog input from 0 to 4.5 V. Five out of six conversion situations (period and timer number) afford plenty of time to convert, average, and store the required eight to ten samples. The saturation samples for the 20 ms period only must be converted in 151 ms, so a leisurely pace is not recommended. With a TCY of 100 ns and an ADCS<5:0> = 2, a TAD of 150 ns can be achieved, resulting in a conversion rate of over 550 ksps. That is a conversion every 1.8 µS, allowing enough time to convert eight to ten samples, average them, and store the average in memory.

The PWM module configuration uses only the PWM1H pin. It sets the time base prescaler, period, and duty cycle in accordance with the active period.

3.7.3 Communication Module Configurations

There are two communication channels supported in this application: an I^2C channel to control the output of the adjustable power supply and an RS232A channel to communicate with a host. With only one master on the bus, the I^2C protocol is uncomplicated. There is no need for clock arbitration, and bus collisions will not occur. The dsPIC is to be configured as the master on this bus, and the AD5259 (in the adjustable power supply) is the slave. The AD5259 is a 7-bit slave, so dealing with the added complexity of a 10-bit address will not be an issue either. The UART module contains two UARTs, but only UART1 is used.

3.8 PIER Final Prototype (PIER II) Assembly and Test

3.8.1 Electrode System

The PIER II electrode system is similar to that used in the PIER I prototype (see Figure 3-8), but implements the two-sensor design shown in Figure 3-47.

The common voltage electrode allows the simultaneous application of pulse voltage to both sensors, while polarization currents are collected through two separated channels. The sensor structure was fabricated by PCB technology on RO3003 substrate (see Figure 3-48), installed between two layers of Teflon®—a 3.5 mm substrate, and a 0.5 mm cover—with epoxy glue.

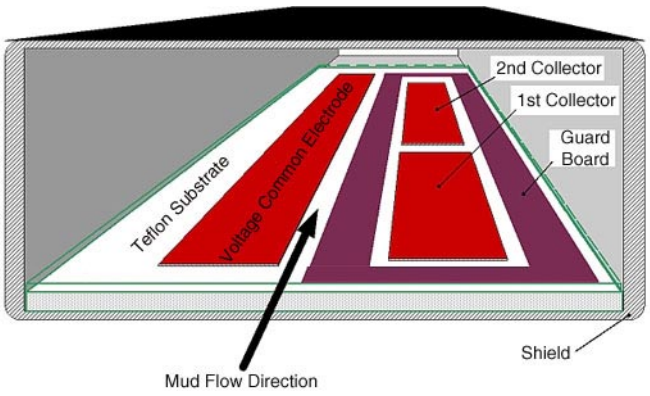


Figure 3-47
Design of PIER electrode section in the protecting shield.

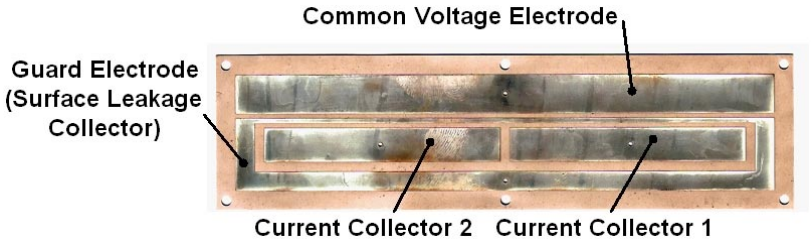


Figure 3-48
Structure of PIER double-sensor electrode structure.

The assembled electrodes were installed on the PIER base with aluminum rivets as shown in Figure 3-49. To prevent mechanical damage and influence of possible electrostatic or electromagnetic fields, the electrode plate is covered by a metal shield. This shield simultaneously organizes the axial flow of mud and depresses the transverse flow from the rotation of the drilling column.

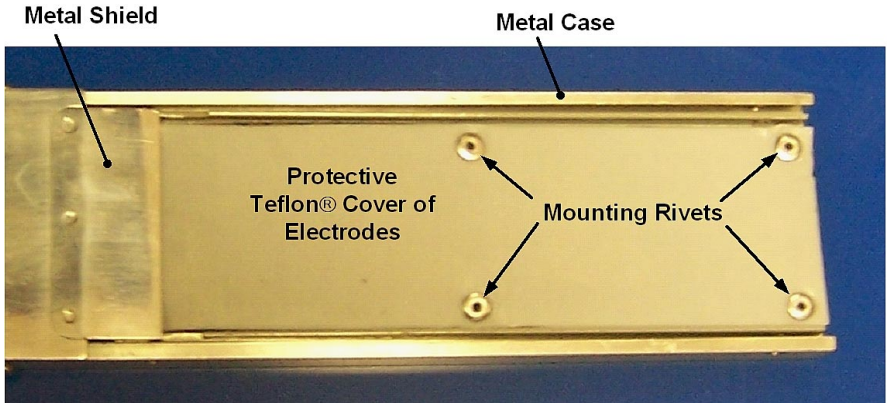


Figure 3-49
PIER sensor module without shielding cover.

3.8.2 Adjustable Power Supply

The adjustable power supply was modified from the initial schematics (see Figure 3-17), thus implementing the variable power source (see Figure 3-50) and generator of voltage pulses (probe driver) that is shown in Figure 3-51.

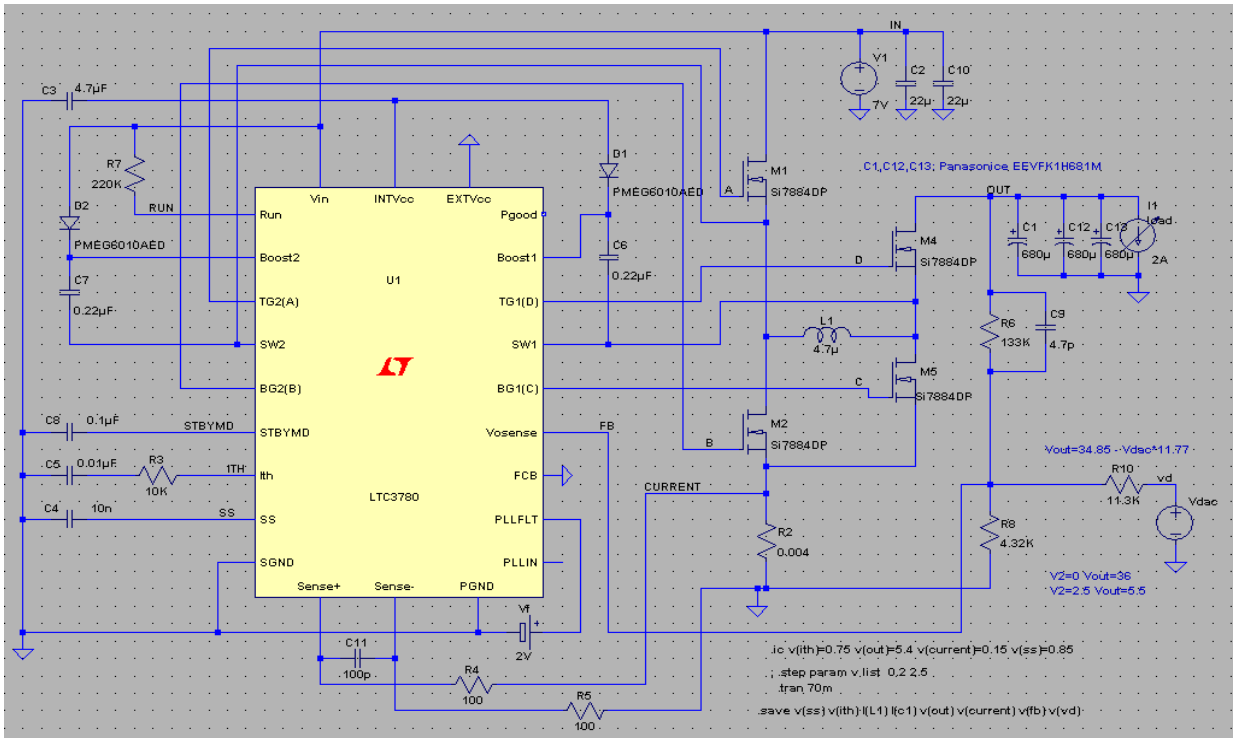


Figure 3-50
Variable power source (0 – 36 V) that is controlled by a microprocessor.

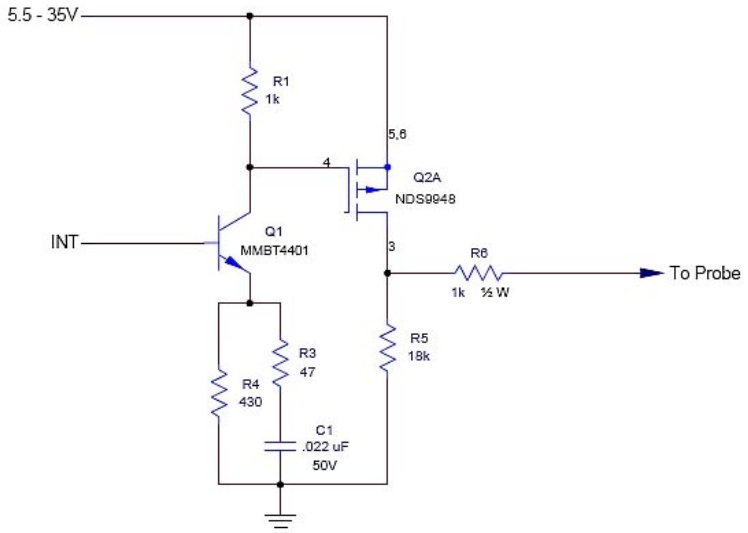


Figure 3-51
Fast voltage switch that generates step-like pulses for the PIER sensor.

We have tested the probe driver at varied power supply voltages. PIER functionality requires an active low edge of INT to turn on the voltage to the probe (see Figure 3-52). That waveform is at the top of each image. The horizontal time base is 25 ns/division. Two output waveforms are shown in each image. The faster one is the output of the probe driver circuit, and the slower one is the voltage across a 500 pF capacitor, intended to simulate the probe. They are separated by a 20 Ω resistor.

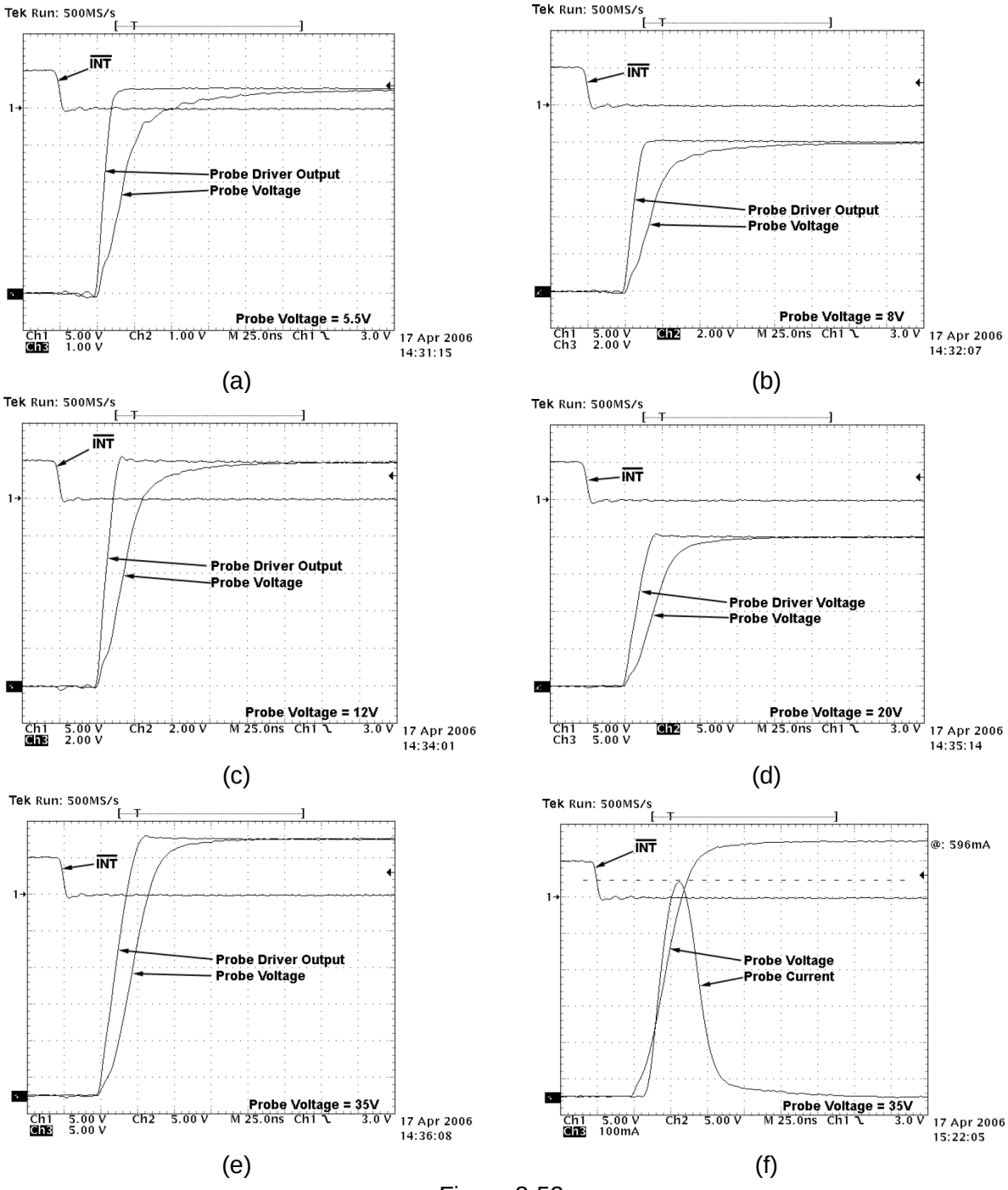


Figure 3-52
Tests of PIER probe driver (voltage step generator): (a), (b), (c), (d) and (e) probe driver voltage output and real step-voltage on the probe for magnitudes of 5.5, 8, 12, 20 and 35 V respectively; (f) probe voltage and current at a magnitude of 35 V.

The probe driver output waveforms for the 5.5 and 8 V samples were measured with an active probe using a 1/3 in. ground lead. Because of the short ground, noise pickup was negligible and the waveform appears quite smooth (except for sampling bobble). Unfortunately, that probe has a voltage range of only ±8 V, so the remainder of the measurements were made using a standard probe with a 4 in. ground lead. Ripple and slight overshoot are apparent in those higher voltage

measurements; however there is no reason to believe that those waveforms are not, in fact, just as noise free as the 5.5 and 8 V waveforms. It is a common measurement error. The probe voltage waveform is taken with a standard probe in all cases. The noise is more obvious at the lower-voltage samples. The oscillograph uses a Tektronix TCP202 50 MHz current probe to measure the charging current through the 500 pF capacitor. Even at a power supply voltage of 35 V, the peak current (displayed by the scope at the dashed line) is only about 600 mA. Lower power supply voltages are correspondingly lower in current.

Most of the delay is attributed to U2, the amplifier that converts the logic level drive of INT- to the 0-5 V drive required by Q2. The remainder of the delay falls on the transistors. The delay contributed by the gate Q1 is negligible. Figure 3-51 presents oscillograms of the probe driver output at different voltage magnitudes.

After the test of the probe driver, a PCB with an adjustable power supply was installed in the corresponding compartment of the PIER base, shown in Figure 3-53.

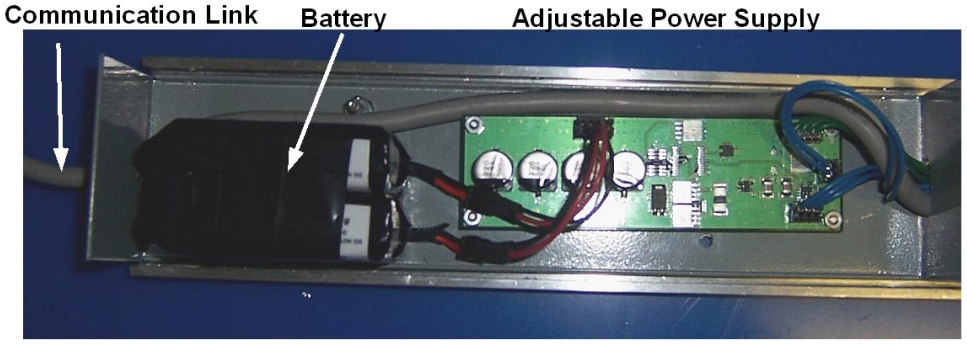


Figure 3-53
Adjustable power supply module of the PIER being installed in the compartment of the PIER base.

3.8.3 Signal Integrator

The double-channel PIER signal integrator was fabricated without modification according to the scheme in Figure 3-17. It is shown in Figure 3-54 with the data acquisition and processing board because they share the same compartment.

3.8.4 Data Acquisition and Processing Board

The fabricated data acquisition and processing board are presented in Figure 3-54.

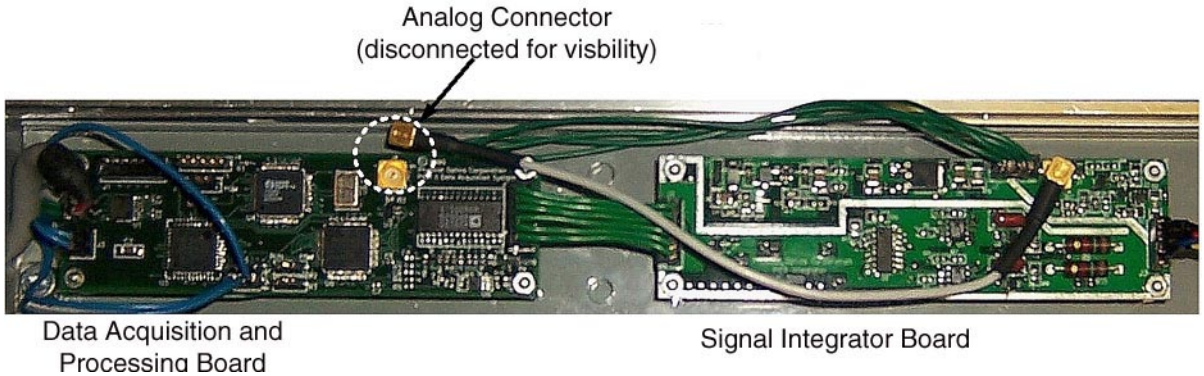


Figure 3-54
Main electronics of the PIER: signal integrator board and data acquisition and processing board, installed in the compartment of the PIER base.

The performance of both boards is discussed in detail in Sections 3.2.4 and 3.3.3. The most challenging part of the printed circuit board (PCB) design for the integrator was the minimalization of the leakage current that corrupts the performance of the integrator. We have solved this problem by implementing a combined structure for the PCB—three internal layers were fabricated from Teflon composite with very low conductivity. Also, to prevent the galvanic interaction of board elements, specifically the DC amplifiers with the integrating op-amp, extended grounded bordering between parts was used. This bordering is clearly visible in Figure 3-54 (signal integrator is on the left).

The detailed schematic of the data acquisition board is shown in Figure 3-55.

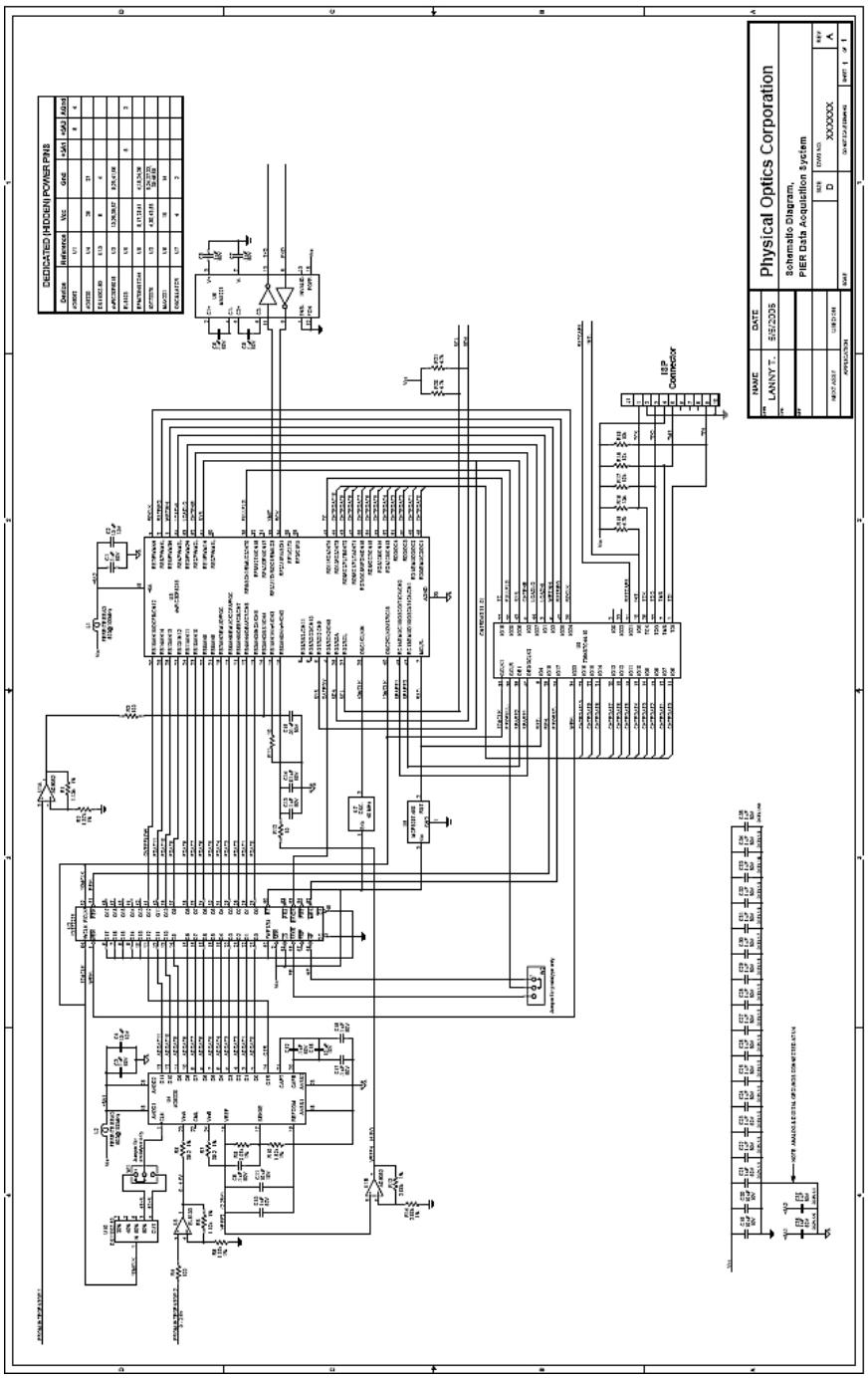


Figure 3-55
PIER data acquisition and processing board scheme.

3.8.5 PIER Assembly and Test

The assembled PIER prototype is shown in Figure 3-56 with open compartments. The completely assembled PIER-II prototype is presented on Figure 1-1.

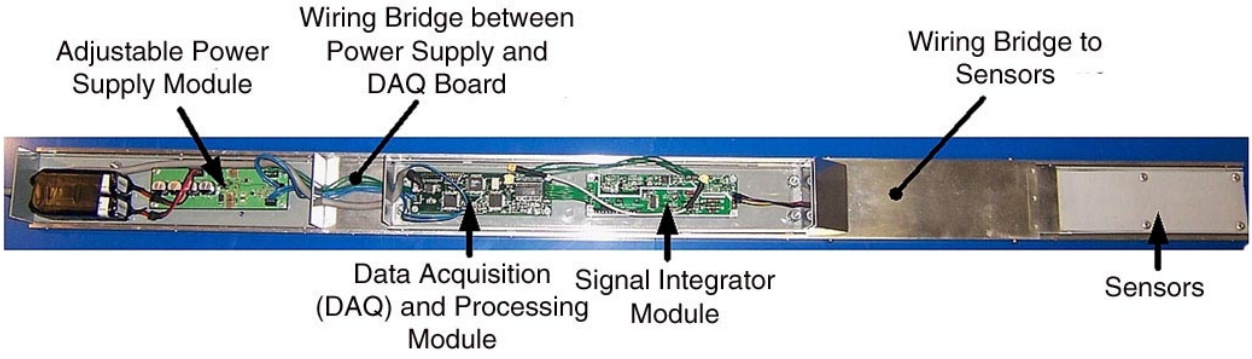


Figure 3-56
PIER II prototype with open compartments.

The PIER prototype was tested with real drilling mud in a laboratory setup that simulates upward mud flow by using a powerful stirrer installed inside the tube (simulating the drilling pipe). This setup is shown in Figure 3-57.

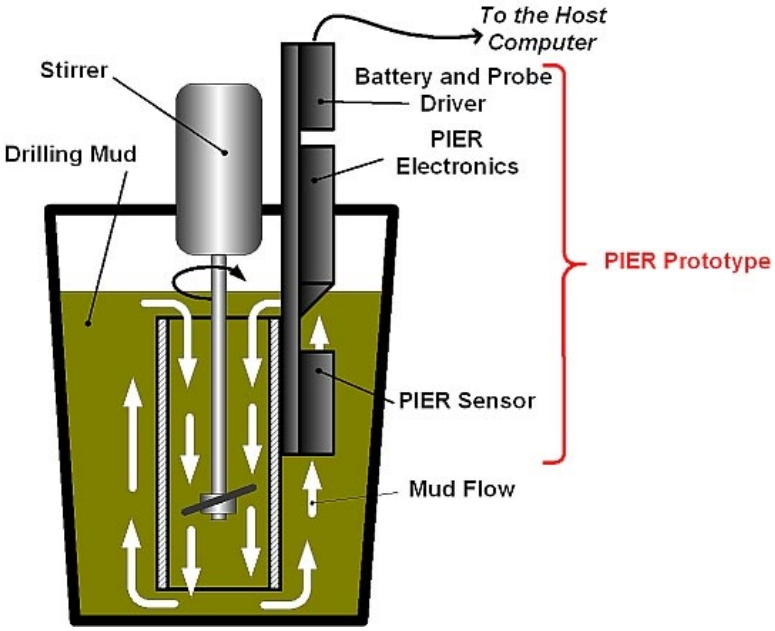


Figure 3-57
PIER prototype final test setup.

The PIER prototype communicated with the host computer through the serial port (RS232); thus we were able to retrieve oil content and mud flow data, as well as spectral data for sensor admittance. The last feature allowed us to control the PIER performance down to the initial measurement data. Due to the high viscosity of the mud, we could not achieve a flow rate of >0.05 ft./s in our laboratory test setup. In this flow rate range we could not detect any influence of the flow on the results of measurements.

Figure 3-58 shows the initial spectrum of dielectric losses in the empty sensor, i.e., the response of the sensor itself. Figures 3-59 and 3-60 present the spectra of dielectric losses during a test of varied oil content in mud, from 0.1% to 10%. The corresponding oil content output is shown in Figure 3-61, where the sensitivity threshold ~1% is clearly observable. All these data demonstrate that the PIER prototype functions as expected and the goal of the project has been met.

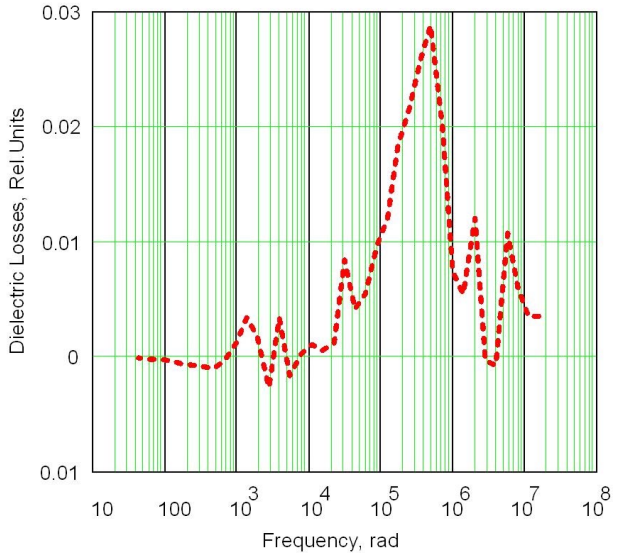


Figure 3-58
Spectrum of dielectric losses in the sensor itself.

This spectrum reflects the polarization losses in the sensor materials and in cables. The peak polarization occurs near 50 kHz. To avoid the influence of these losses on the calculation of oil content, the polarization data of the empty sensor are recorded and subtracted from measurement data in the time domain. Figures 3-59 shows spectra of dielectric losses in the varied compositions of mud and oil both for initial data and after the subtraction of the sensor polarization.

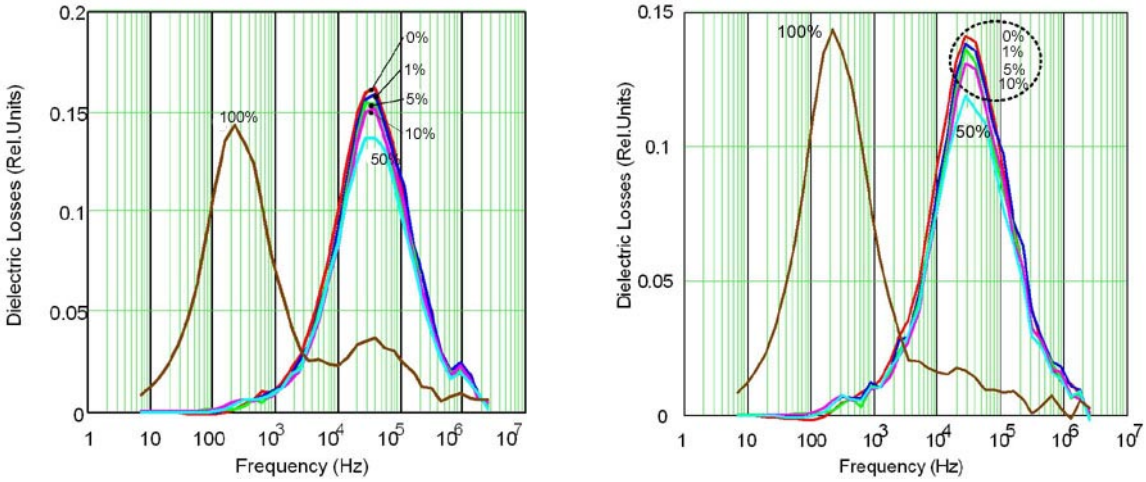


Figure 3-59
Spectra of dielectric losses in the mud with different oil contents:
before (a) and after (b) subtraction of sensor polarization.

Comparison of the spectra in Figures 3-59(a) and (b) demonstrates that the high-frequency peak for pure oil is the result of sensor influence, and it disappears after the data correction. Due to the conductivity of the mud, the molecular polarization of the oil is very weak in the mixture, but it is still measurable as shown in Figure 3-60.

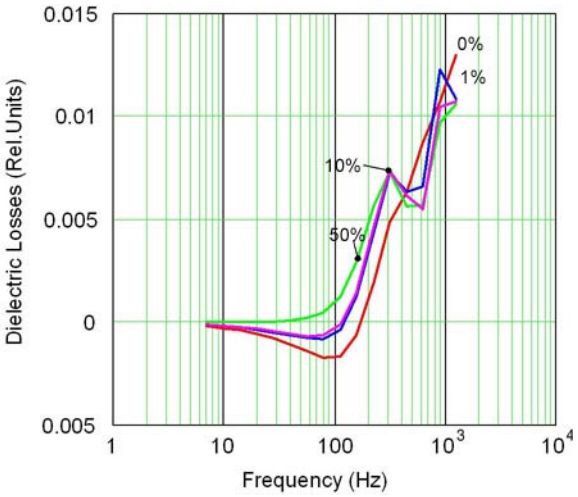


Figure 3-60
Low-frequency dielectric losses in the mud with different oil contents: Peak dielectric losses at 200 Hz are observable for all samples excluding pure mud.

Low molecular polarization of the oil in the composition with conductive mud is the result of electrostatic shielding of oil droplets. Thus the influence of oil content is the imterfacial polarization of these droplets in the conductive medium (mud). This polarization decreases the average electric field in the composition, thus decreasing the high-frequency polarization of the mud-filled sensor (peak at 30 kHz). The relative decrement of this peak, $(A_m - A_c)/A_m$, where A_m and A_c are magnitudes of losses peak at 30 kHz for pure mud and composite respectively, was used as a parameter that presents the oil content. The dependence of this parameter on the real oil content, used in tests, is shown in Figure 3-61.

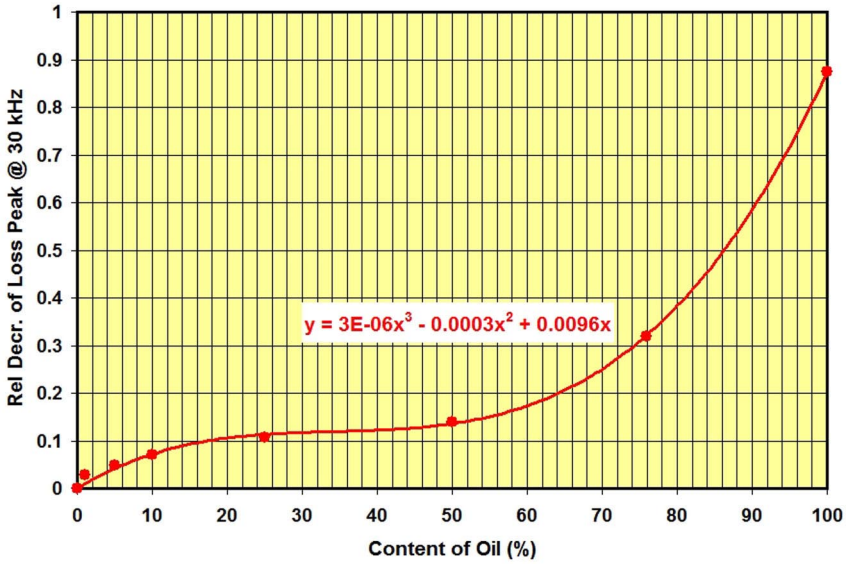


Figure 3-61
PIER output data versus the real oil content.

The dependence of the measured parameter on the oil content is clearly nonlinear and may be presented in simplified form as $y \approx 0.0003x(32 - x + 0.01x^2)$. The change of the concavity (inflection point) reflects the transition from the mixture of oil in mud (low oil content) to a mixture of mud in oil (high oil content). In practice, a calibration curve like presented in Figure 3-61 has to be determined for the mud used. Nevertheless, any decrement of the polarization losses in the drilling mud has to be considered as the penetration of the low-conductive substance (oil) in the drilling well.

3.9 Applications and Commercial Scenarios for the PIER Technology

This section was prepared with the help of Foresight Science & Technology as a part of the DOE commercialization assistance program.

3.9.1 Market

The market niche identified for initial commercial entry is described in Table 3-7.

Table 3-7. Description of Market Niche

Name	Petroleum Exploration/ Oilfield Service Sector
Initial Impression of Market Driver(s) Identified for the Next 5 Years	In the drilling and measurement market, technical drivers include the need to deal with increasingly severe environmental conditions including sourer crudes and higher temperatures [12]. Other technical concerns involve "adapting sensor technology and logging to hot, deep wells [12]." There also seem to be very strong and continuous economic drivers to keep drilling costs as low as possible. Discovery costs are a constant economic driver for solutions that allow those costs to be curbed [13].
Initial Impression of Key End-User Needs	The biggest challenge ahead will be making sure that remote equipment such as satellites used for monitoring well progress, and the downhole sensors that relay data to them, are durable and that their performance is repeatable and reliable. The goal is to achieve greater production efficiency without making the downhole environment so complex as to invite unreliable results or outright equipment failure [13]. High-cost wells, especially offshore or in harsh environments, will benefit the most from intelligent completions via downhole tools. In the future, the industry will be able to combine subsurface gauges and distributed fiber-optic sensors and actuators downhole.
Initial Impression of Adequacy of Current Technology to Address those Needs	There does not appear to be a similar technology capable of duplicating the performance of this technology.
Price of Substitutable Products if Any	There does not appear to be a substitutable product on the marketplace. There are downhole sensors but none that provide the type of information the sensor from Physical Optics expects to provide.
Market Size	Industry experts estimate that the total market size for oilfield equipment and machinery is around 1.1 billion and growing at about 10% annually [14]. By 2009, the drilling equipment market is expected to account for 40% of the $13 billion North American oil and gas field machinery market [15].

The commercial scenario analyzed is the licensing of PIER technology to a commercial partner who can integrate it into their data logging system. The technology is a downhole sensor that would be used in conjunction with other measurement-while-drilling systems used by petroleum drilling companies. The key innovation will be the capability of the device to measure downhole oil concentration during drilling and instantly relay that information to the surface. Current alternatives require that the mud be returned to the surface before oil concentrations can be measured.

Foresight Science & Technology has contacted experts to gauge their views on the PIER technology's potential competitiveness in general. These findings are summarized below.

1. *Importance of Need(s) Being Addressed:* An important need is potentially being addressed. Although the oil concentration in the mud can be measured when it is returned to the surface, it appears that PIER technology will offer the capability to get that concentration measurement instantaneously. The technology would be another informational tool for the rig engineer.
2. *Key Specifications and Characteristics to Emphasize for this Niche:* There are several key specifications to emphasize in this niche. First, and potentially foremost, is the capability of the technology to handle the extreme stresses it will be placed under in a downhole application. This will include extreme pressure, high vibration, and extreme temperatures. Key performance specifications will be the technology's ability to operate in particularly harsh conditions with very high heat and extreme pressure. A second area that logging operators might be particularly interested in will be the sensitivity of the instrument.
3. *Price and Pricing Factors for This Niche:* The price will depend on the performance and usefulness of the technology to logging operations. The price depends on the value proposition to the oil company; i.e., if the key innovation is real-time information about the content of the mud, then the price would need to depend on how important getting that information quickly would be. Experts suggest that regardless of who manufactures the sensor, the oil drilling company doing MWD will strongly prefer to license the technology or else buy the technology outright as a possible alternative.
4. *Potential Competitiveness of Technology:* The technology sounds novel and appears to meet a key need; therefore, it should be very competitive. The competitiveness, like the potential price, depends on the value PIER is providing to the oil driller. If real-time information is important, then the technology sounds very competitive.
5. *Who Are the Key Competitors:* To the best of our and surveyed experts' knowledge, no technologies like this currently are available in logging operations, and we have not heard of anyone doing something similar.
6. *Who Are Likely Targets:* Schlumberger, Halliburton, and the consulting companies providing drilling services are the likely targets. Triton Engineering is another company that might have an interest in the technology. Other targets are Weatherford and Baker-Hughes. But any technology would be put through rigorous paces in order to meet these logging companies' standards. These companies, like Schlumberger and Halliburton, either manufacture their own equipment or license equipment from outside vendors. In this, licensing was the likely commercialization scenario, regardless of whether Physical Optics was the manufacturer or not. If these companies do not initially decide to license the technology, then they would move to acquire it if there was strong interest. The integration would be a key issue, but the licensor would handle the integration and, in fact, would likely demand to do so in order to ensure they had complete knowledge and control over the downhole operation.

Given this analysis, the value proposition for this technology is as follows:

The technology offers the potential to provide constant information about the concentration of oil in drilling mud during the drilling process. The sensor can also measure the drilling mud flow rate. Typically, a drill operator must wait until the drilling mud returns to the surface before measuring the oil concentration in the drilling mud. The technology would allow this measurement to be made in real time in the downhole.

3.9.2 Competition

On Google and RaDiUS, under the terms "measurement while drilling," "logging while drilling," "downhole sensor," "downhole measurement," "well logging," and "mud logging," we conducted a search for relevant products, patents, and projects. The results are summarized in Tables 3-8 and 3-9.

Table 3-8. Examples of Relevant Products/Services Identified

Product Name	***Manufacturer***	***Relevance***	***Web Site/Phone***
NaviTrak® II	Baker-Hughes INTEQ,	Described as the benchmark for measurement while drilling. The tool uses a mud pulse telemetry system to transmit information about "real-time inclination, azimuth, toolface reference and tool temperature [16]."	http://www.bakerhughes.com/inteq/evaluation/mwd/navitrak2.htm 202-785-8093
Measurement-While-Drilling/ Logging-While-Drilling Services	Sperry Drilling Services-Halliburton	"A complete line of LWD services is available from Sperry Drilling Services, utilizing both mud pulse and electromagnetic telemetry. Data can be transmitted in real time or recorded in downhole memory and retrieved after each bit run after the tool returns to the surface. Parameters vital for real-time applications and decisions are selected for transmission. Meanwhile, the remaining raw data, diagnostic parameters, and other information is recorded in downhole memory and accessed at the end of each bit run [17]."	http://www.halliburton.com/esg/sd1318.jsp 281-988-2557
Pulse Telemetry & Surveying	Schlumberger	Schlumberger has a variety of different MWD and LWD tools to assist in drilling. The company also has a technology called E Pulse XR, an electromagnetic MWD service [18].	http://www.slb.com/content/services/drilling/lwd/index.asp 212-350-9400
Sensors (Standard) Mud System	International Logging	According to the company Website, International Logging's equipment can do the following: • Pit level • Mud conductivity (in and out) • Mud density (in and out) • Mud temperature (in and out) • Mud flow out • Pump SPM [19]	http://www.inter-log.com/standard_equip.htm 713-849-1800
Monitor SWD	Gyrodata	"MONITOR™ is a mud-pulse telemetry directional measurement system for tracking deviation while drilling vertical wells. Run by the rig crew, MONITOR obtains and transmits accurate, real-time inclination, azimuth, and tool face measurements to the surface. MONITOR™ also has the ability to provide tool-face readings in the event a well needs to be corrected back to vertical using a bent housing motor [20]."	http://www.gyrodata.com/ 713-461-3146

Table 3-9. Examples of Relevant Projects Identified

Project Title	***Performing Institution***	***Performance Period***	***Relevance***
"Downhole spectrometric device for the real time analysis of fluid composition"	Hanby Environmental Lab Procedures	Jul. 2003 to Apr. 2004	No abstract of this project was provided, only the title. The following excerpt is from Hanby's Web site: "The Hanby method offers a revolutionary solution to obtaining on-site samples that potentially contain petroleum-related substances. ….. The Hanby method is designed to provide a precise color indication of the concentration of petroleum (gasoline, diesel, crude oil, etc.) in field samples."
"Surface Instrumentation for Downhole Event Recognition"	Noble Technology Services Division, Noble Corporation	Up to March 2006	"Maurer Technology completed a project sponsored by the U.S. Department of Energy to develop and test an instrumented data-acquisition sub that is mounted in a drill string below the top drive and used to detect downhole events. Data recorded at the surface during drilling operations would then be processed and presented to the driller to discern undesirable drilling conditions and help optimize drilling rates and maximize the life of components in the BHA. Four series of field tests of the surface instrumentation system were conducted throughout the effort… The sub was designed to collect hook load, rotary torque, rotary speed, rotary position, drill pipe pressure, mud temperature, triaxial vibration, and triaxial magnetometer data."
"Preliminary Testing of a Novel Downhole Fiber Optic Fluid Analyzer"	Martin E. Cobern, SPE & William E. Turner, APS Technology, Inc.; John Cooper & Jeffrey F. Aust, Old Dominion University	Presented at the 2000 SPE/DOE Improved Oil Recovery Symposium	"A novel fiber optic downhole fluid analyzer has been developed for real-time determination of the oil, gas and water fractions of fluids from different zones in a multizone or multilateral completion environment. A near-infrared attenuation measurement provides differentiation among oil, water, and gas at all but the highest water cuts. An induced fluorescence measurement unambiguously determines the oil fraction of the fluid as a validity check on the attenuation measurement. The only downhole components of the system are the fiber optic cable, lenses, and windows, which may be installed in multiple locations in the well and operated with a single surface unit."
Deep Geophysical Observatory in Long Valley Caldera	Carnegie Institution of Washington	Aug. 2000 to Jul. 2004	This award was granted in support of the development of an integrated downhole sensor package for use in making geophysical observations in the Long Valley Caldera.

The following patent mapping, conducted using Delphion, indicates there may be competing technology. When we searched the term "downhole sensor," we got 121 hits among filed patents and applications. The leader was Baker Hughes with 25 hits, followed by Shell Oil with 15 and Halliburton with 7 hits. Schlumberger was next with 6 hits. Some of the smaller players in the field include Sensor Highway Limited, Baroid Technology Inc., Hughes Tool Company, Atlantic Richfield, Pangaea Enterprises, Inc. The highest number of these hits, 26, were filed in the year 2001 followed closely by 2002, which had 24 hits. 2003 had 10 hits, 2004 had 8, 2005 had 2 and 2006 had 2, so filing activity appears to have died down recently. Others are researching and developing technology that may become a threat within the next 5 years.

Thus the projects uncovered did not appear to be similar enough to PIER technology to judge them to be real potential threats, and it appears as though there is not a technology similar to PIER currently in use. Schlumberger appears to be the industry leader and they manufacture or control many of the measurement drilling tools they utilize. The other larger drilling companies, Halliburton, Baker Hughes, and Weatherford appear to have some of their own measurement technology and license the rest of their technologies from other vendors. Given the harsh environmental conditions to which downhole equipment can be exposed, there does appear to be an element of brand loyalty, trust, and goodwill in the industry.

Schlumberger appears unique in the field in that they produce all their measurement- and logging-while-drilling technologies from within or through outright acquisitions. The other majors, like Halliburton or Baker Hughes take a combinatorial approach, developing some of their own tools and licensing tools from third-party suppliers.

3.9.3 Targets

The target here is the organization that will partner with POC to commercialize PIER technology. There are feasible and viable targets. Feasible targets have relevant product lines and appear to have an established presence in the market. Viable targets, unless otherwise noted, are those that still appear to be good candidates if they have their potential interest in the PIER technology. We seek viable targets that appear to be in good financial health, are established in the market with a relevant product line, can provide capabilities that are relevant for commercializing this technology, and possess good absorptive capacity. Identified targets are presented in Table 3-10.

POC or Foresight Science & Technology contacted all of these companies to determine their potential interest in licensing or acquiring the downhole sensor technology from POC. Based on these conversations, we think there are at least two feasible entry strategies to get the technology to the major players and also second-tier companies in the drilling service and measurement field. A direct strategy would be through Schlumberger, where they would acquire the technology outright. POC has already begun this strategy through our previous contact with Schlumberger. They have the capabilities and desire to manufacture their own tools for use. An alternative strategy is to sell to the other major players in the drilling services field like Halliburton or Baker Hughes through their measurement-while-drilling tool suppliers. These third-party suppliers, mentioned in Table 3-10, often sell to multiple vendors, both large and small, within the industry. We have contacted several of them and solidified strong interest from one, APS Technologies. APS Technologies has excellent manufacturing capabilities, already manufactures sensor and measurement technology, and counts Halliburton and Baker Hughes among their current clients. APS sells equipment to other smaller drilling service companies and also to companies involved in directional drilling. APS Technologies also has extensive experience in telemetry technology and in transmitting information from downhole sensors to the surface. They also have an existing testing facility that could help prove PIER technology. The contact person at APS Technologies is Martin Coburn, Vice President of Research and Development. His contact information is mcobern@aps-tech.com or he can be reached at 860-613-4450.

Table 3-10. Potential Targets for Partnership with POC to Commercialize PIER Technology

Name of Company or Unit and Address	Name, Title, Phone, and E-mail of Point of Contact	Web Site	Reason for Recommending
Gyrodata 1682 W. Sam Houston Pkwy. N. Houston, Texas 77043	Gary Uttecht, garyu@gyrodata.com	http://www.gyrodata.com/index.htm	Gyrodata manufactures a variety of drilling equipment including survey-while-drilling systems.
APS Technology 800 Corporate Row, Cromwell, CT 06416-2072	Martin E. Cobern Vice President, Research and Development	http://www.aps-tech.com/company/index.html	"APS Technology designs, develops, and manufactures electromechanical assemblies, sensors, and hardware to operate under severe conditions. Working environments include: long-term vibration, shocks, high temperature and pressure, caustic fluids, abrasive wear, harmful gases or any combination thereof."
International Logging, Inc. 6550 W. Sam Houston Pkwy N., Suite 250 Houston, TX 77041	Bill Henderson	http://www.inter-log.com/equipment.htm	A company devoted entirely to mud logging.
Triton Engineering/Noble Technology Services Division 13135 South Dairy Ashford, Suite 800 Sugar Land, Texas 77478-3686	Gerry Pittard – Noble Downhole Technology 281-276-6100 gpittard@noblecorp.com	http://www.triton-services.com/About/Overview.asp	Noble Downhole Technology Corporation was founded with the purpose of investing in downhole technologies that would improve Noble's core operations.

3.9.4 Examples of Relevant Deals

Table 3-11. Relevant Deals

Parties	Key Terms	Date
Luna Innovations and Baker Hughes	These two parties formed a joint venture, Luna Energy, in 2002 to develop fiber optic sensor systems for oil and gas exploration. A current development project at Luna Energy is a dedicated fiber-optic-based well-monitoring system for real-time intelligent well production optimization and permanent monitoring applications.	Early 2002
Verdisys Horizontal Technology	A 2005 license agreement between Edge Capital Group and Verdisys, a company licensing down-hole equipment for petroleum exploration. According to the terms of the agreement, the "Licensee will pay licensor $2,500 per well drilled and ten (10) percent pre-tax revenue generated by the rig as cash is received from oil & gas well revenue. Licensee will pay Licensor a royalty of five (5) percent of pre-tax revenue as cash is received from oil & gas revenue generated by the use of the License and on other rigs manufactured or leased by Licensee."	2005

The second deal is particularly relevant for PIER technology, especially given the fact that the technology is a piece of down-hole equipment.

The key issue is the performance of the sensor both in terms of qualitative results and in terms of its ability to tolerate environmental stresses. The environmental stresses of a downhole are severe enough and are only exacerbated by the technology working during continuous drilling. Therefore, some sort of rigorous testing and performance program will need to be built into the deal. A testing program should be implemented to ensure that the technology proves its capability prior to commercial use. APS Technologies has the capabilities to help POC thoroughly test the technology to verify its performance in extreme environmental conditions.

3.9.5 Term Sheet Considerations for Licensing

Industry Average Royalty Rate. According to John Pyrdol, an economist at the Department of Energy who specializes in the oil and gas industry, standard royalty rates for the industry are 12.5% of gross receipts for drilling on federal lands and 16.66% when drilling offshore on a platform. We also contacted Yiorgos Kostoulas from the MIT Technology Licensing Office. Mr. Kostoulas is a licensing expert who specializes in materials science: semiconductors, optics, materials, robotics, and instrumentation and has experience licensing technology in the oil and gas industry. Mr. Kostoulas suggested that the royalty rate be based upon a 25% percent rule; that is, POC would get a 25% royalty on the cost savings due to the installation of PIER sensors.

Initiation Fees if Any. Given the upfront risks and unproven nature of the technology, an initiation fee may be difficult to command. Though they may not be easy to obtain, initiation fees may be possible, as we saw in the Verdisys Horizontal Technology deal mentioned above. This may be a point to hash out in negotiations with APS Technologies.

Warrantees, if Any. We think this may be an issue that will arise given the stresses the technology will eventually be placed under. This may be handled under the existing contract APS Technologies may have with their customers for their own downhole technology. We expect that if the technology were sold through APS Technologies, then PIER technology would be covered under the existing warranty terms of the contract they have with the drilling services company.

4.0 CONCLUSIONS

During the Phase II contract, POC performed all needed tasks and met all objectives of the project. We developed, fabricated, and tested the PIER Phase II prototype (PIER II), which includes the battery-powered probe driver, dual capacitive sensor (probe), analog charge-sensitive signal amplifier, data digitizing, acquisition and processing electronics, and the communication port. We analyzed (together with Foresight Science & Technology, Providence, RI) possible applications and commercialization scenarios.

Testing of the PIER Phase II prototype demonstrated that oil content in drilling mud can be determined with a sensitivity threshold of ~1% (as was suggested in Phase I). This is the natural limitation of available electrode structures with fluctuation levels because of the flow rate of the mud. The PIER design eliminates the influence of mud flow on measurement, instead converting this challenge to a useful feature such as flow rate measurement. The embedded microcontroller handles the full data acquisition and processing schedule, thus providing real-time indication of the oil content and flow rate. At the same time, the dielectrometric spectrum data can be retrieved for analytic issues other than oil content (for example, salinity of the mud).

We expect to expand the possibilities of the PIER hardware and software by the engineering design of the rugged case to the sensor and integration with the logging system used by

customers during the commercialization of this project, in accordance with two identified entry strategies for the commercialization of PIER technology. Commercialization of this technology will contribute to the full exploitation of oil deposits, thus promoting the U.S. energy independence.

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